FIG. 1

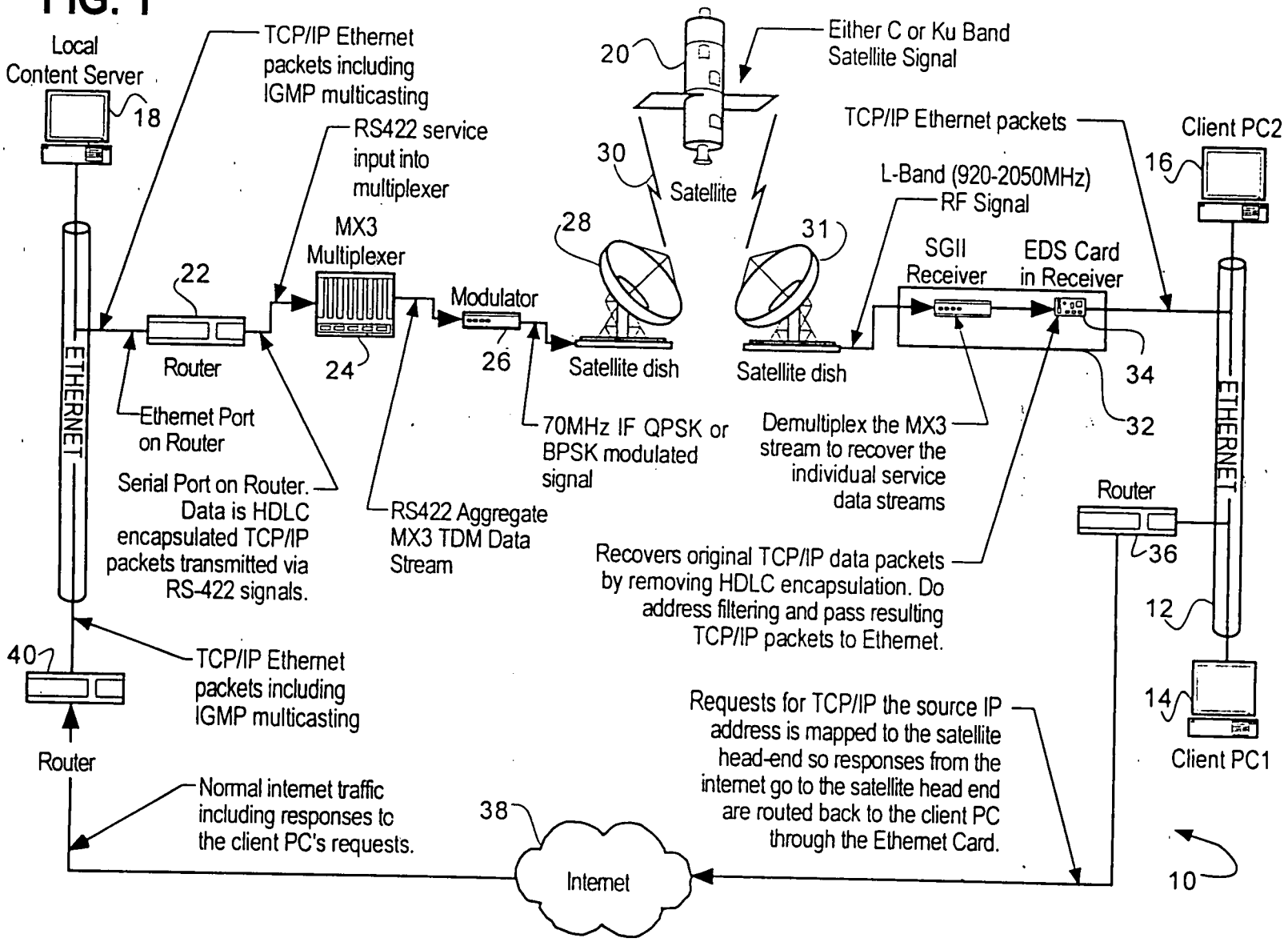

Local Content Server
18
TCP/IP Ethernet packets including IGMP multicasting
RS422 service input into multiplexer
MX3 Multiplexer
22
24
Modulator
26
Router
Ethernet Port on Router
Serial Port on Router. Data is HDLC encapsulated TCP/IP packets transmitted via RS-422 signals.
RS422 Aggregate MX3 TDM Data Stream
70MHz IF QPSK or BPSK modulated signal
ETHERNET
40
TCP/IP Ethernet packets including IGMP multicasting
Router
Normal internet traffic including responses to the client PC's requests.
38
Internet
20
Either C or Ku Band Satellite Signal
30
Satellite
28
Satellite dish
31
Satellite dish
TCP/IP Ethernet packets
L-Band (920-2050MHz) RF Signal
SGII Receiver
EDS Card in Receiver
34
32
Demultiplex the MX3 stream to recover the individual service data streams
Recovers original TCP/IP data packets by removing HDLC encapsulation. Do address filtering and pass resulting TCP/IP packets to Ethernet.
Requests for TCP/IP the source IP address is mapped to the satellite head-end so responses from the internet go to the satellite head end are routed back to the client PC through the Ethernet Card.
Client PC2
16
Router
36
ETHERNET
12
14
Client PC1
10

FIG. 2

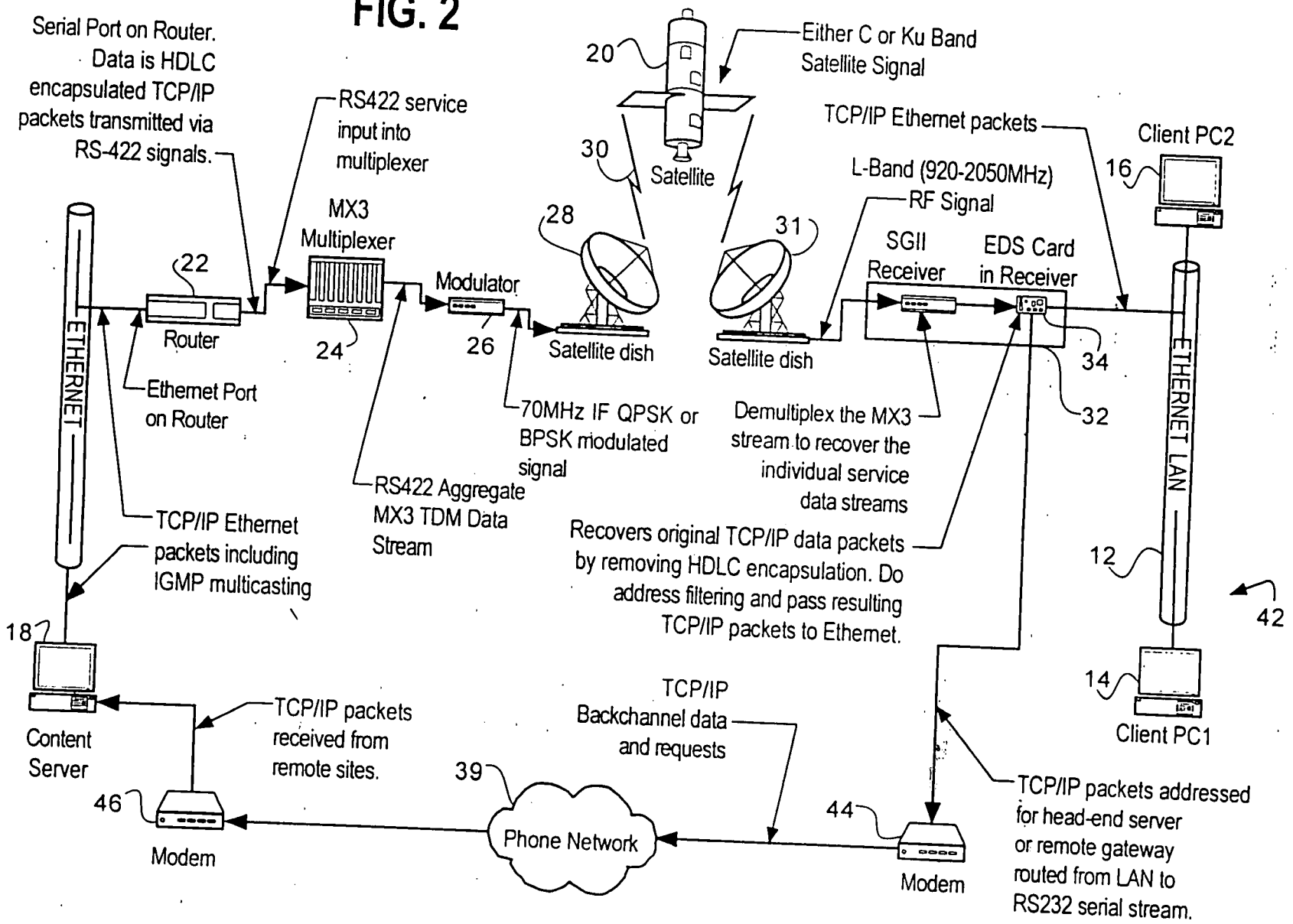

Serial Port on Router. Data is HDLC encapsulated TCP/IP packets transmitted via RS-422 signals.
RS422 service input into multiplexer
20
Either C or Ku Band Satellite Signal
TCP/IP Ethernet packets
Client PC2
16
30
Satellite
L-Band (920-2050MHz) RF Signal
MX3 Multiplexer
28
31
SGII Receiver
EDS Card in Receiver
22
Modulator
ETHERNET
Router
24
26
Satellite dish
Satellite dish
34
ETHERNET LAN
Ethernet Port on Router
70MHz IF QPSK or BPSK modulated signal
Demultiplex the MX3 stream to recover the individual service data streams
32
RS422 Aggregate MX3 TDM Data Stream
TCP/IP Ethernet packets including IGMP multicasting
Recovers original TCP/IP data packets by removing HDLC encapsulation. Do address filtering and pass resulting TCP/IP packets to Ethernet.
12
42
18
14
Content Server
TCP/IP packets received from remote sites.
TCP/IP Backchannel data and requests
Client PC1
39
46
44
Phone Network
Modem
Modem
TCP/IP packets addressed for head-end server or remote gateway routed from LAN to RS232 serial stream.

FIG. 3
PRIOR ART

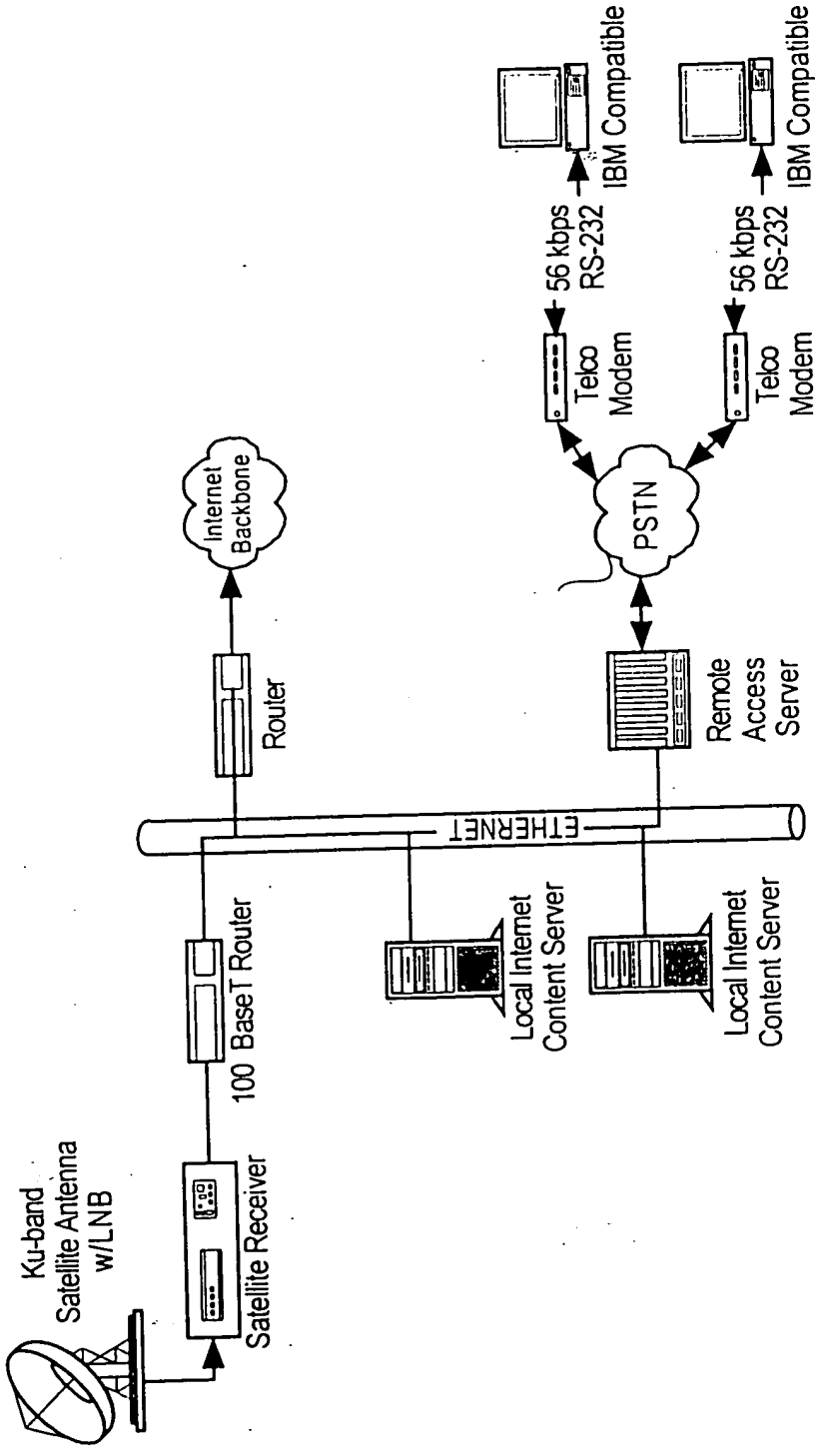


FIG. 4

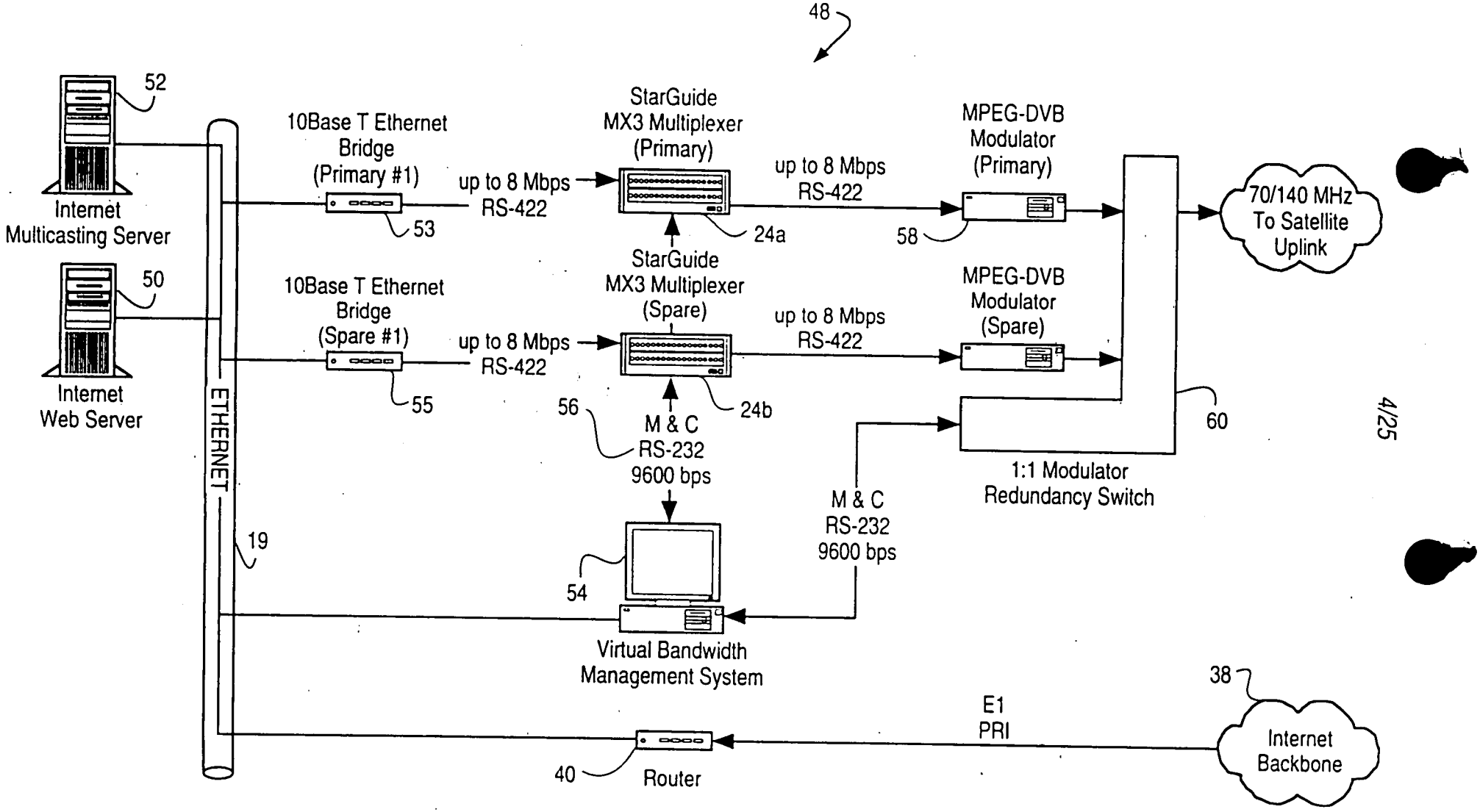

48
52
Internet
Multicasting Server
50
Internet
Web Server
ETHERNET
19
10Base T Ethernet
Bridge
(Primary #1)
53
up to 8 Mbps
RS-422
StarGuide
MX3 Multiplexer
(Primary)
24a
up to 8 Mbps
RS-422
MPEG-DVB
Modulator
(Primary)
58
70/140 MHz
To Satellite
Uplink
10Base T Ethernet
Bridge
(Spare #1)
55
up to 8 Mbps
RS-422
StarGuide
MX3 Multiplexer
(Spare)
24b
up to 8 Mbps
RS-422
MPEG-DVB
Modulator
(Spare)
56
M & C
RS-232
9600 bps
60
1:1 Modulator
Redundancy Switch
M & C
RS-232
9600 bps
54
Virtual Bandwidth
Management System
38
E1
PRI
Internet
Backbone
40
Router

FIG. 5

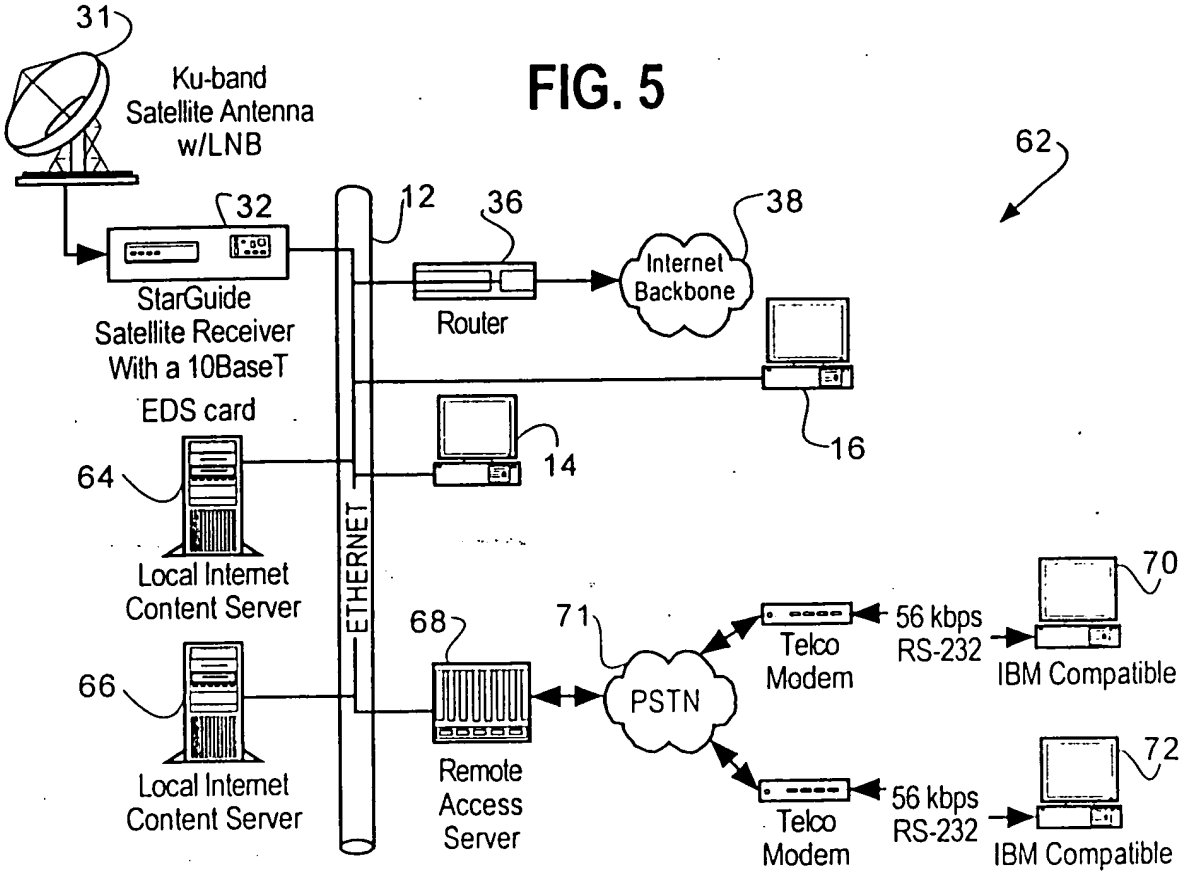

31
Ku-band
Satellite Antenna
w/LNB
32
StarGuide
Satellite Receiver
With a 10BaseT
EDS card
12
36
Router
38
Internet
Backbone
62
16
14
64
Local Internet
Content Server
ETHERNET
66
Local Internet
Content Server
68
Remote
Access
Server
71
PSTN
Telco
Modem
56 kbps
RS-232
70
IBM Compatible
Telco
Modem
56 kbps
RS-232
72
IBM Compatible

FIG. 6

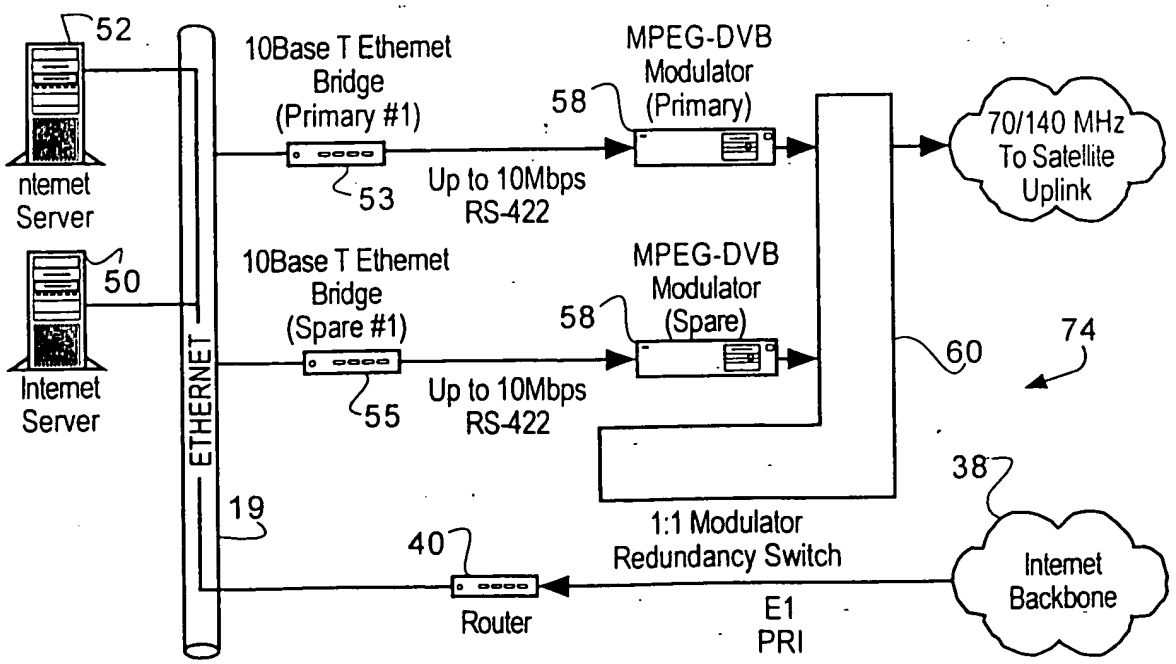

52
nternet
Server
50
Internet
Server
ETHERNET
19
10Base T Ethernet
Bridge
(Primary #1)
53
Up to 10Mbps
RS-422
MPEG-DVB
Modulator
(Primary)
58
70/140 MHz
To Satellite
Uplink
10Base T Ethernet
Bridge
(Spare #1)
55
Up to 10Mbps
RS-422
MPEG-DVB
Modulator
(Spare)
58
60
74
1:1 Modulator
Redundancy Switch
38
Internet
Backbone
40
Router
E1
PRI

FIG. 7

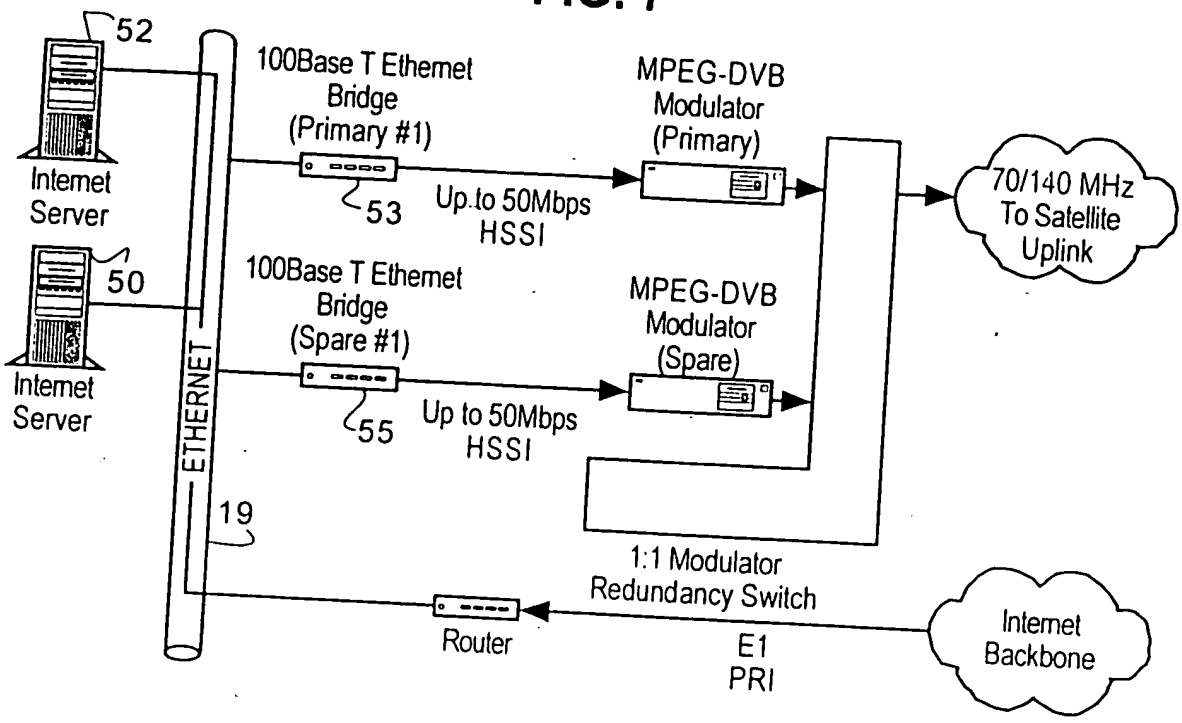

52
Internet Server
50
Internet Server
ETHERNET
19
100Base T Ethernet Bridge (Primary #1)
53
Up to 50Mbps HSSI
MPEG-DVB Modulator (Primary)
70/140 MHz To Satellite Uplink
100Base T Ethernet Bridge (Spare #1)
55
Up to 50Mbps HSSI
MPEG-DVB Modulator (Spare)
1:1 Modulator Redundancy Switch
Router
E1 PRI
Internet Backbone

FIG. 8

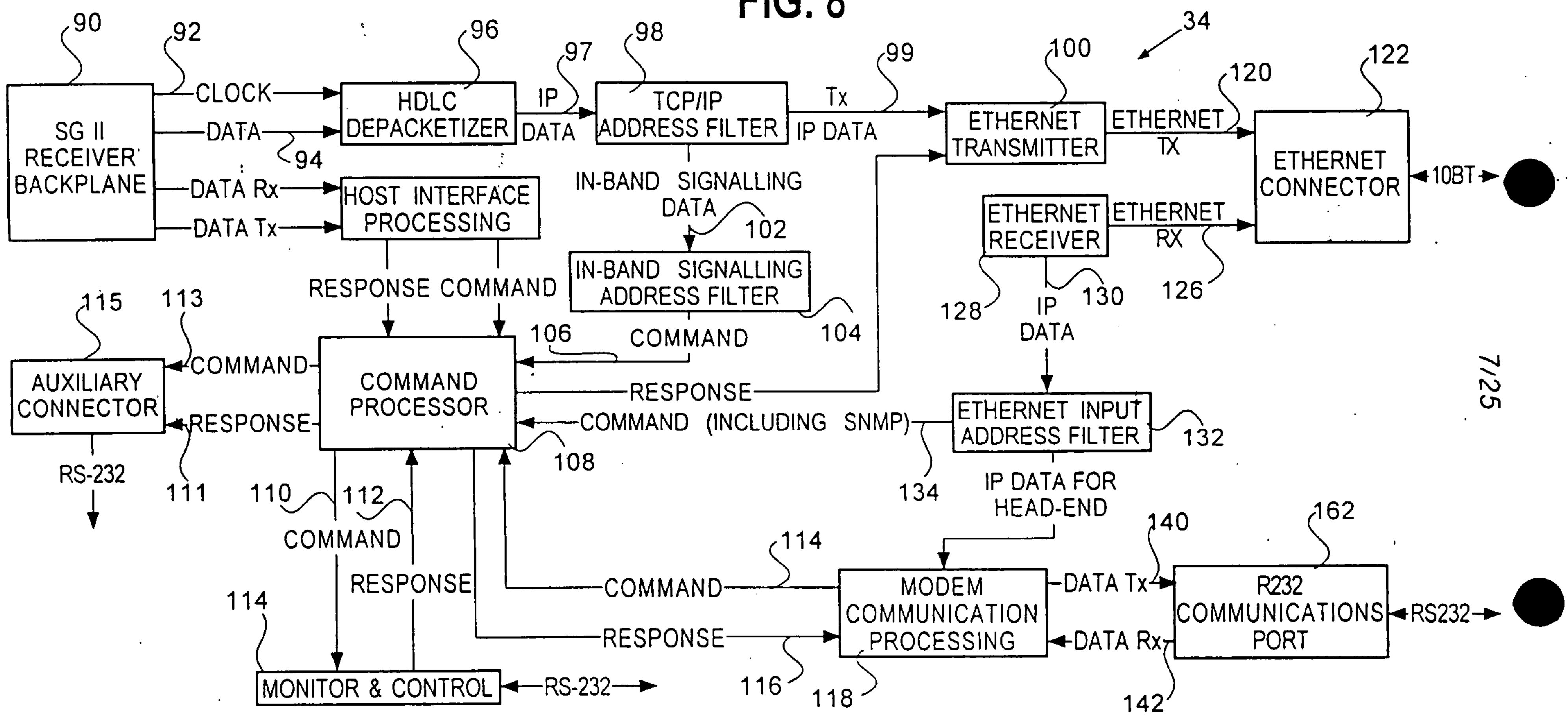
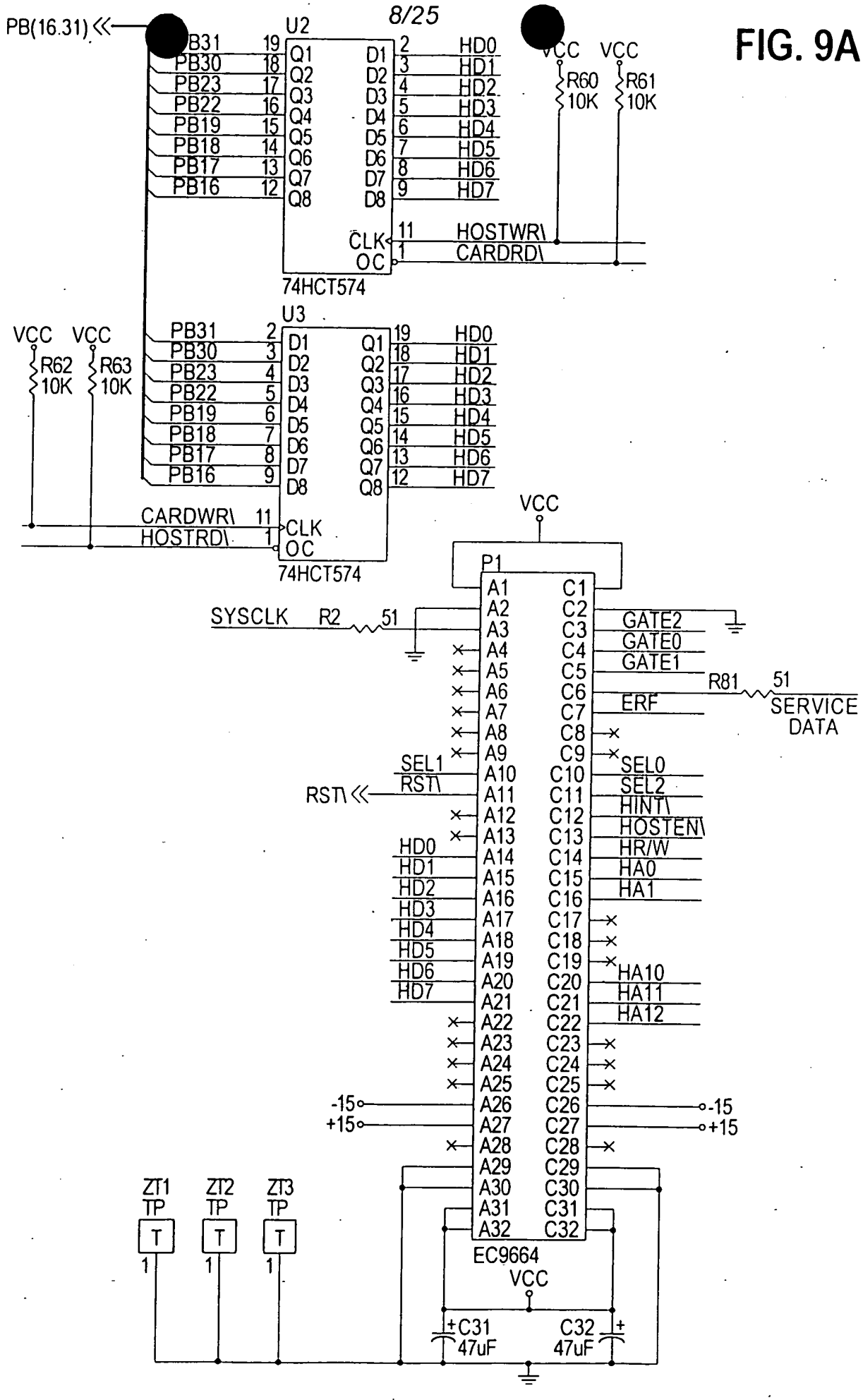

34
90
SG II RECEIVER BACKPLANE
92
CLOCK
DATA
94
DATA Rx
DATA Tx
96
HDLC DEPACKETIZER
97
IP DATA
98
TCP/IP ADDRESS FILTER
99
Tx IP DATA
100
ETHERNET TRANSMITTER
120
ETHERNET TX
122
ETHERNET CONNECTOR
10BT
HOST INTERFACE PROCESSING
RESPONSE
COMMAND
IN-BAND SIGNALLING DATA
102
IN-BAND SIGNALLING ADDRESS FILTER
104
COMMAND
106
ETHERNET RECEIVER
128
130
ETHERNET RX
126
IP DATA
115
AUXILIARY CONNECTOR
113
COMMAND
RESPONSE
111
RS-232
COMMAND PROCESSOR
RESPONSE
COMMAND (INCLUDING SNMP)
108
134
ETHERNET INPUT ADDRESS FILTER
132
IP DATA FOR HEAD-END
110
112
COMMAND
RESPONSE
114
COMMAND
114
MODEM COMMUNICATION PROCESSING
RESPONSE
116
118
140
DATA Tx
DATA Rx
142
162
R232 COMMUNICATIONS PORT
RS232
MONITOR & CONTROL
RS-232

FIG. 9A


PB(16.31)
U2
PB31 19
PB30 18
PB23 17
PB22 16
PB19 15
PB18 14
PB17 13
PB16 12
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 8
D8 9
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
CLK 11
OC 1
HOSTWR\
CARDRD\
74HCT574
VCC
VCC
R60
10K
R61
10K
U3
VCC
VCC
R62
10K
R63
10K
PB31 2
PB30 3
PB23 4
PB22 5
PB19 6
PB18 7
PB17 8
PB16 9
D1
D2
D3
D4
D5
D6
D7
D8
Q1 19
Q2 18
Q3 17
Q4 16
Q5 15
Q6 14
Q7 13
Q8 12
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
CARDWR\ 11
HOSTRD\ 1
CLK
OC
74HCT574
VCC
P1
SYSCLK
R2
51
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
A30
A31
A32
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
GATE2
GATE0
GATE1
R81
51
SERVICE DATA
ERF
SEL1
RST\
SEL0
SEL2
HINT\
HOSTEN\
HR/W
HA0
HA1
HA10
HA11
HA12
-15
+15
-15
+15
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
RST\
ZT1
TP
ZT2
TP
ZT3
TP
T
1
EC9664
VCC
C31
47uF
C32
47uF

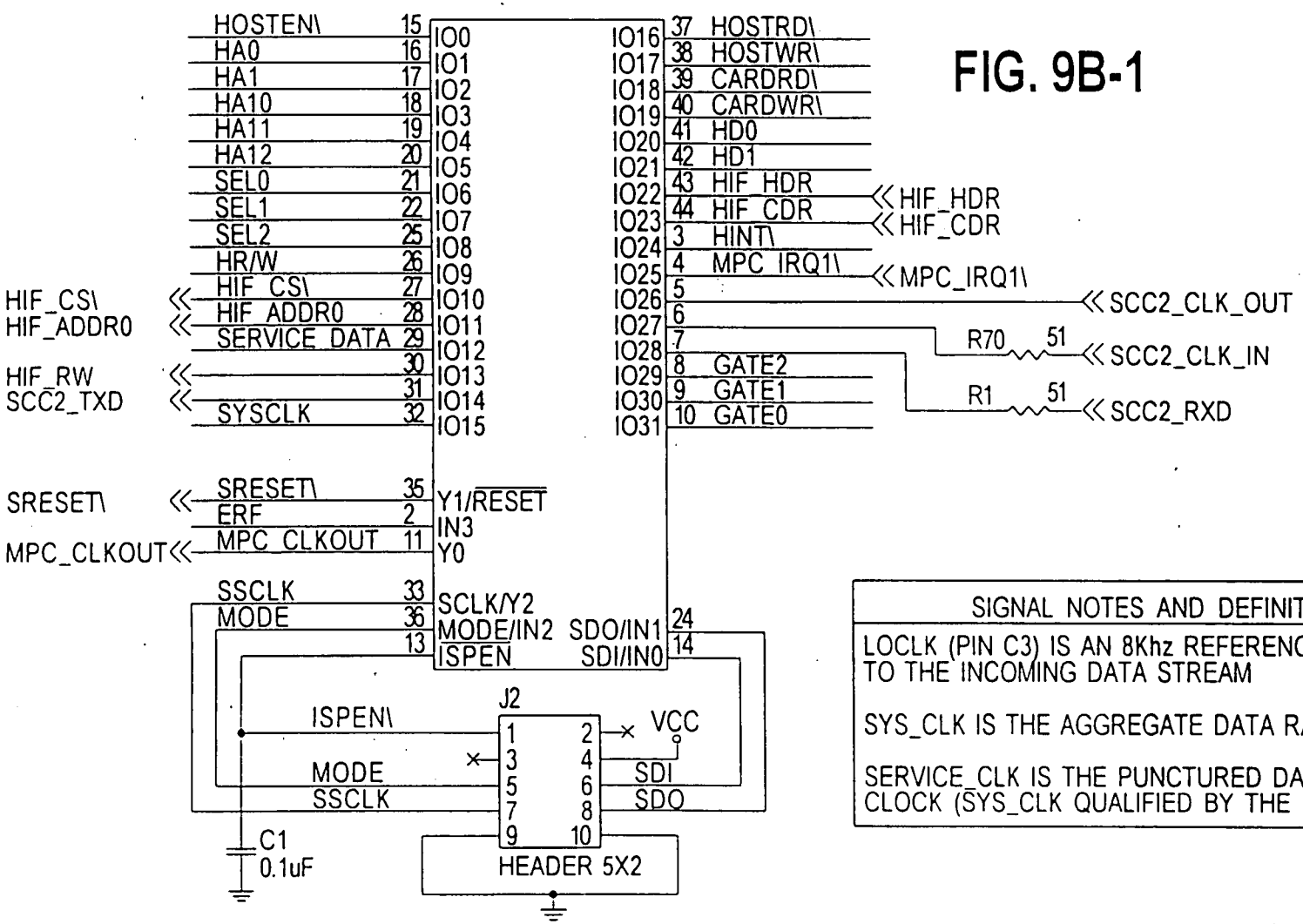
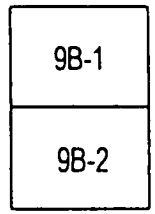


FIG. 9B-1

FIG. 9B



SIGNAL NOTES AND DEFINITIONS
LOCLK (PIN C3) IS AN 8Khz REFERENCE LOCKED TO THE INCOMING DATA STREAM SYS_CLK IS THE AGGREGATE DATA RATE. SERVICE_CLK IS THE PUNCTURED DATA RATE CLOCK (SYS_CLK QUALIFIED BY THE GATE SIGNAL).

FIG. 9B-2

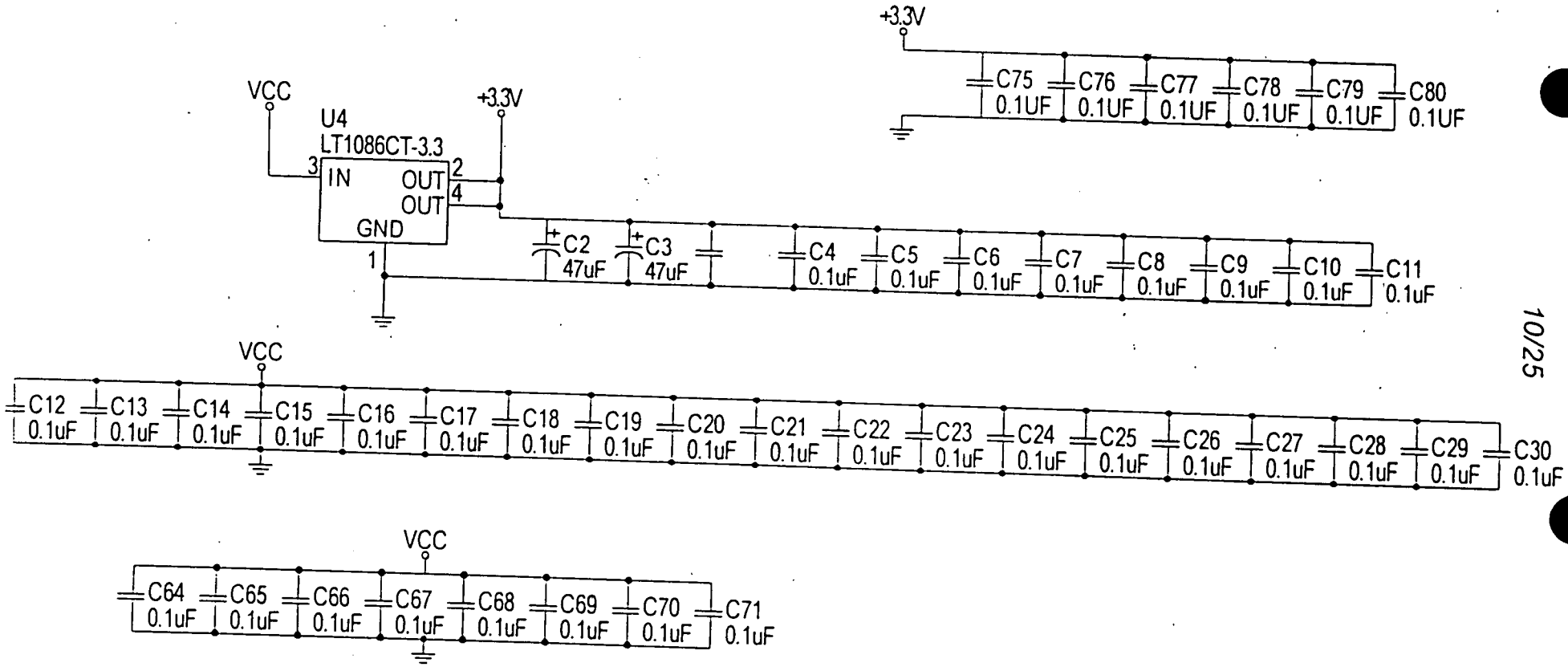

+3.3V
C75 0.1UF
C76 0.1UF
C77 0.1UF
C78 0.1UF
C79 0.1UF
C80 0.1UF
VCC
U4
LT1086CT-3.3
3
IN
OUT
2
OUT
4
GND
1
+3.3V
C2 47uF
C3 47uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
VCC
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C30 0.1uF
VCC
C64 0.1uF
C65 0.1uF
C66 0.1uF
C67 0.1uF
C68 0.1uF
C69 0.1uF
C70 0.1uF
C71 0.1uF

FIG. 10A

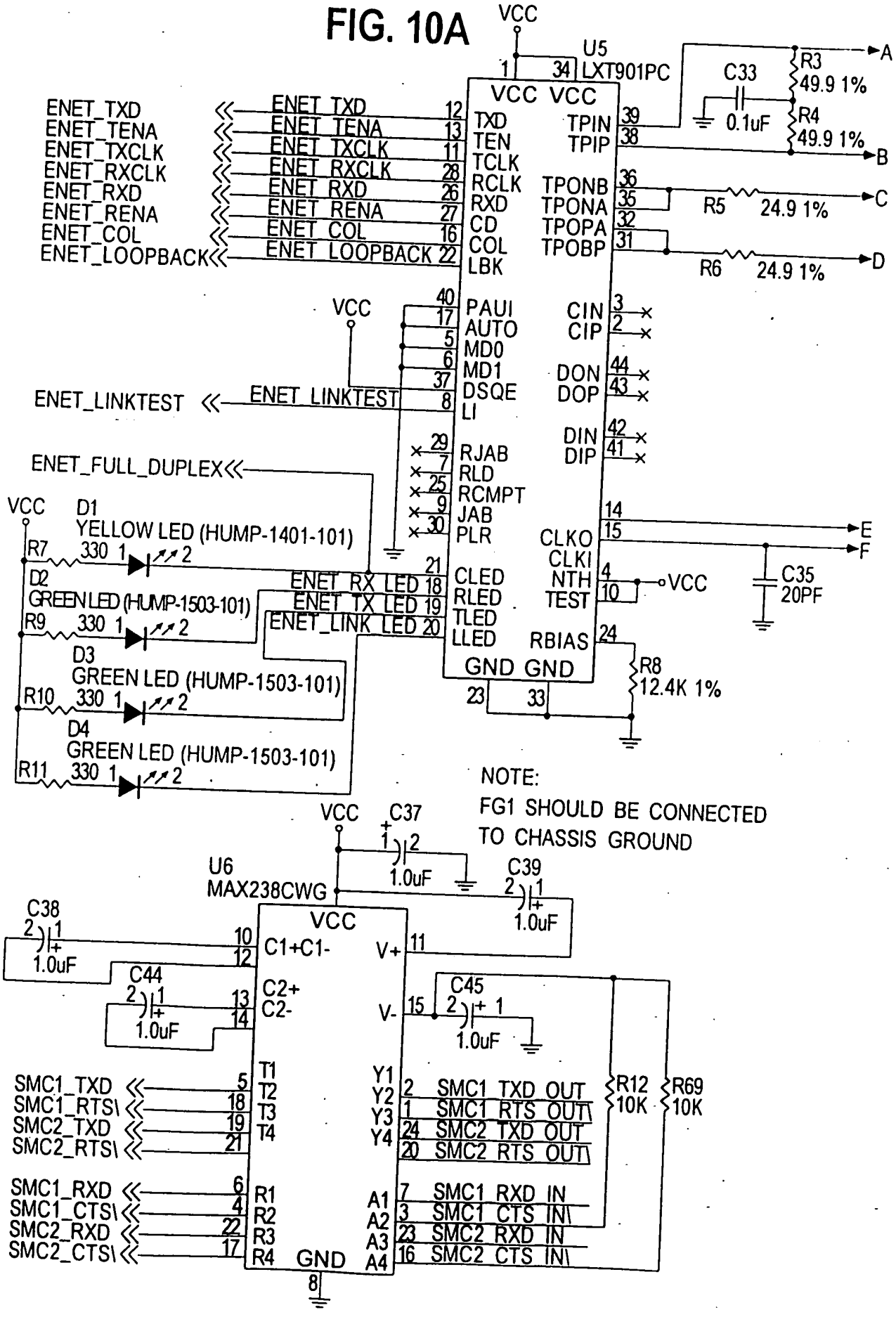
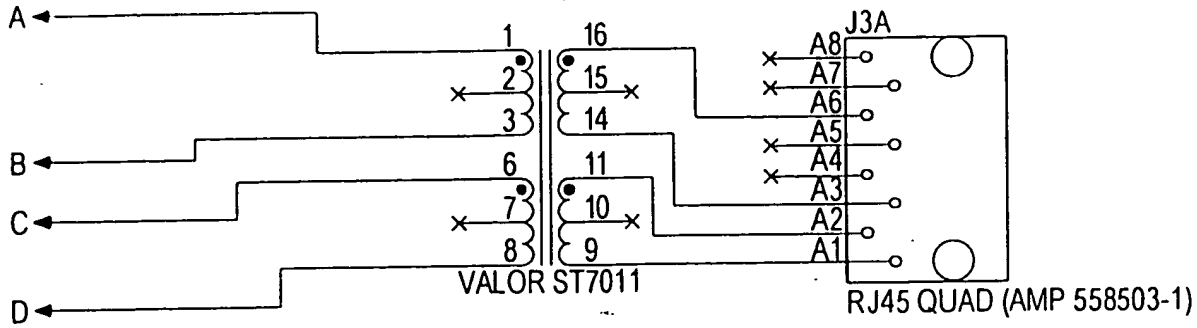
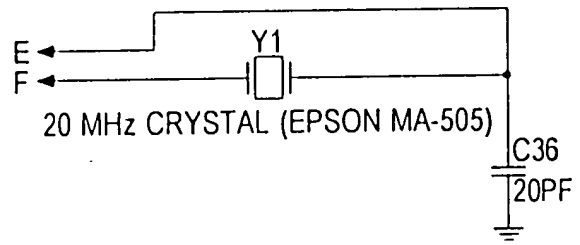
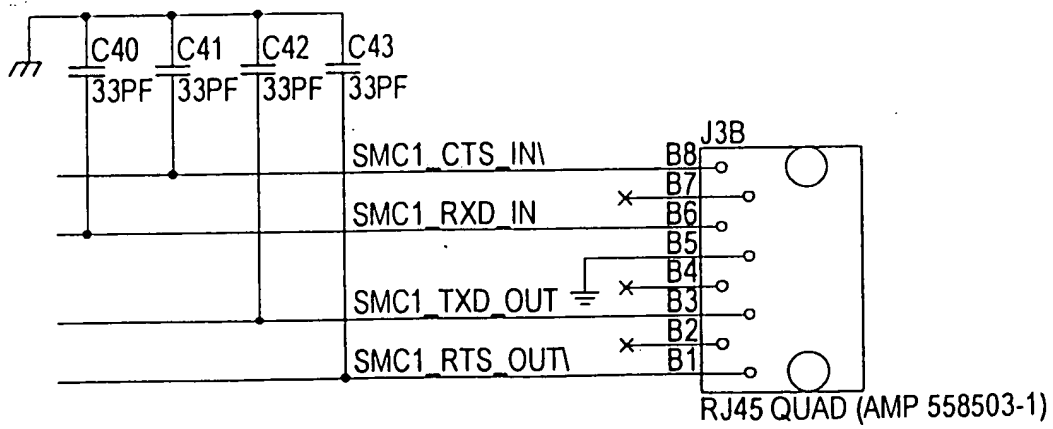

VCC
U5
LXT901PC
ENET_TXD
ENET_TENA
ENET_TXCLK
ENET_RXCLK
ENET_RXD
ENET_RENA
ENET_COL
ENET_LOOPBACK
TXD
TEN
TCLK
RCLK
RXD
CD
COL
LBK
TPIN
TPIP
TPONB
TPONA
TPOPA
TPOBP
C33
0.1uF
R3
49.9 1%
R4
49.9 1%
R5
24.9 1%
R6
24.9 1%
A
B
C
D
PAUI
AUTO
MD0
MD1
DSQE
LI
RJAB
RLD
RCMPT
JAB
PLR
CIN
CIP
DON
DOP
DIN
DIP
CLKO
CLKI
NTH
TEST
RBIAS
ENET_LINKTEST
ENET_FULL_DUPLEX
ENET_RX_LED
ENET_TX_LED
ENET_LINK_LED
CLED
RLED
TLED
LLED
GND
D1
YELLOW LED (HUMP-1401-101)
D2
GREEN LED (HUMP-1503-101)
D3
GREEN LED (HUMP-1503-101)
D4
GREEN LED (HUMP-1503-101)
R7
R9
R10
R11
330
R8
12.4K 1%
C35
20PF
E
F
NOTE:
FG1 SHOULD BE CONNECTED
TO CHASSIS GROUND
U6
MAX238CWG
C37
C38
C39
C44
C45
1.0uF
C1+
C1-
C2+
C2-
V+
V-
T1
T2
T3
T4
R1
R2
R3
R4
Y1
Y2
Y3
Y4
A1
A2
A3
A4
SMC1_TXD
SMC1_RTS\
SMC2_TXD
SMC2_RTS\
SMC1_RXD
SMC1_CTS\
SMC2_RXD
SMC2_CTS\
SMC1 TXD OUT
SMC1 RTS OUT\
SMC2 TXD OUT
SMC2 RTS OUT\
SMC1 RXD IN
SMC1 CTS IN\
SMC2 RXD IN
SMC2 CTS IN\
R12
10K
R69
10K

FIG. 10B



VALOR: ST7011
HALO: TG42-1406N1
BELFUSE: S553-0716





IBM COMPATIBLE PC RS-232 DB-9 MALE PINOUT:
PIN 2 - RX INPUT TO PC
PIN 3 - TX OUTPUT FROM PC
PIN 5 - GROUND
PIN 7 - RTS OUTPUT FROM PC
PIN 8 - CTS INPUT TO PC

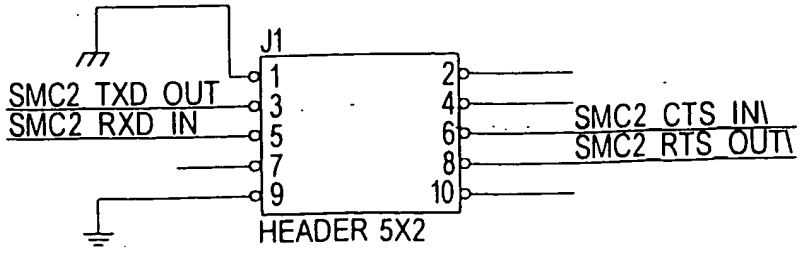


FIG. 11A

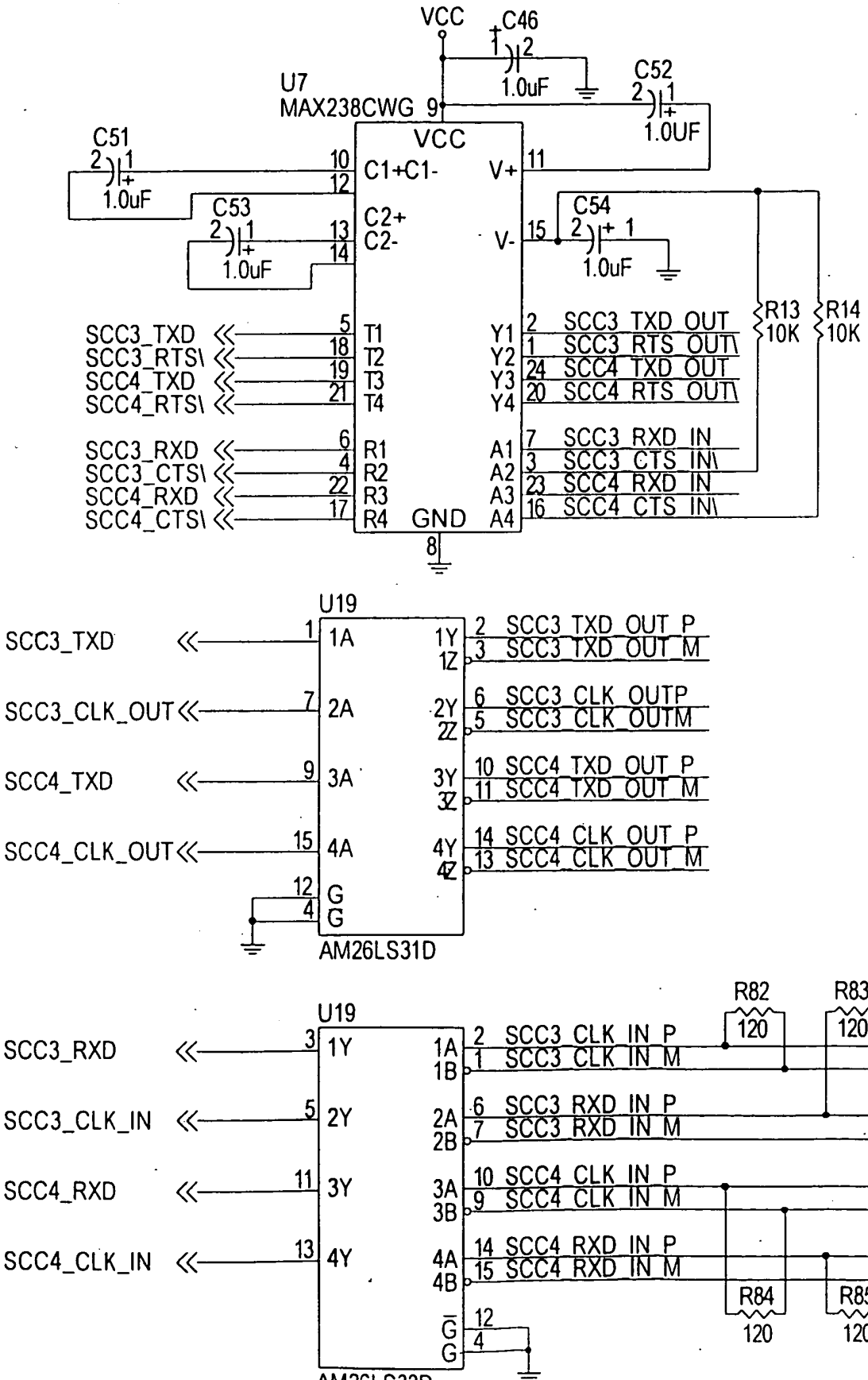

VCC
C46
1.0uF
C52
1.0UF
U7
MAX238CWG
VCC
C1+C1-
V+
C2+
C2-
V-
C51
1.0uF
C53
1.0uF
C54
1.0uF
SCC3_TXD
SCC3_RTS\
SCC4_TXD
SCC4_RTS\
SCC3_RXD
SCC3_CTS\
SCC4_RXD
SCC4_CTS\
T1
T2
T3
T4
R1
R2
R3
R4
GND
Y1
Y2
Y3
Y4
A1
A2
A3
A4
SCC3 TXD OUT
SCC3 RTS OUT\
SCC4 TXD OUT
SCC4 RTS OUT\
SCC3 RXD IN
SCC3 CTS IN\
SCC4 RXD IN
SCC4 CTS IN\
R13
10K
R14
10K
U19
SCC3_TXD
SCC3_CLK_OUT
SCC4_TXD
SCC4_CLK_OUT
1A
2A
3A
4A
G
G
1Y
2Y
3Y
4Y
SCC3 TXD OUT P
SCC3 TXD OUT M
SCC3 CLK OUTP
SCC3 CLK OUTM
SCC4 TXD OUT P
SCC4 TXD OUT M
SCC4 CLK OUT P
SCC4 CLK OUT M
AM26LS31D
U19
SCC3_RXD
SCC3_CLK_IN
SCC4_RXD
SCC4_CLK_IN
1Y
2Y
3Y
4Y
G
G
1A
1B
2A
2B
3A
3B
4A
4B
SCC3 CLK IN P
SCC3 CLK IN M
SCC3 RXD IN P
SCC3 RXD IN M
SCC4 CLK IN P
SCC4 CLK IN M
SCC4 RXD IN P
SCC4 RXD IN M
R82
120
R83
120
R84
120
R85
120
AM26LS32D

FIG. 11B

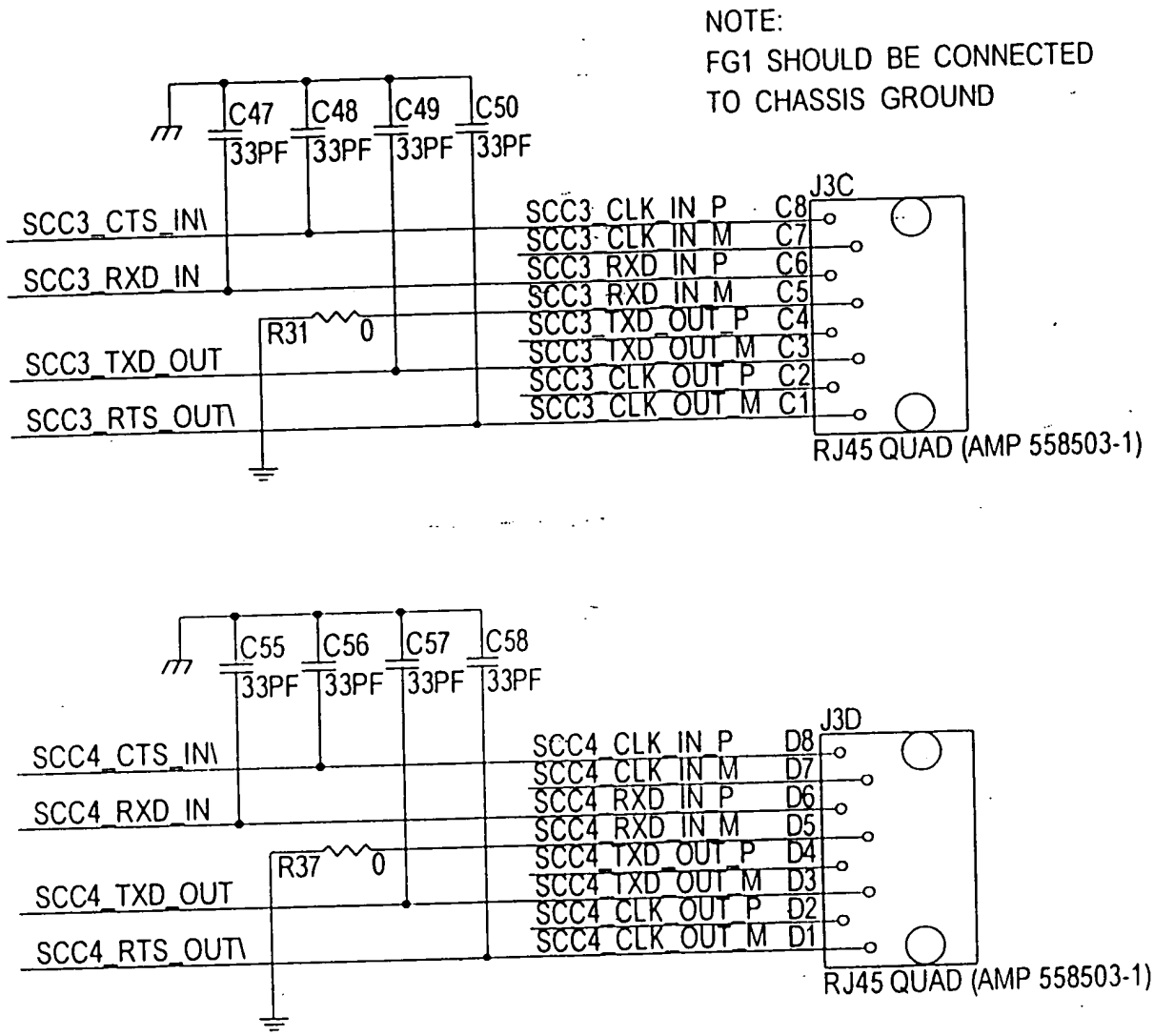

NOTE:
FG1 SHOULD BE CONNECTED
TO CHASSIS GROUND
C47 33PF
C48 33PF
C49 33PF
C50 33PF
SCC3_CTS_IN\
SCC3_RXD_IN
R31 0
SCC3_TXD_OUT
SCC3_RTS_OUT\
J3C
SCC3_CLK_IN_P C8
SCC3_CLK_IN_M C7
SCC3_RXD_IN_P C6
SCC3_RXD_IN_M C5
SCC3_TXD_OUT_P C4
SCC3_TXD_OUT_M C3
SCC3_CLK_OUT_P C2
SCC3_CLK_OUT_M C1
RJ45 QUAD (AMP 558503-1)
C55 33PF
C56 33PF
C57 33PF
C58 33PF
SCC4_CTS_IN\
SCC4_RXD_IN
R37 0
SCC4_TXD_OUT
SCC4_RTS_OUT\
J3D
SCC4_CLK_IN_P D8
SCC4_CLK_IN_M D7
SCC4_RXD_IN_P D6
SCC4_RXD_IN_M D5
SCC4_TXD_OUT_P D4
SCC4_TXD_OUT_M D3
SCC4_CLK_OUT_P D2
SCC4_CLK_OUT_M D1
RJ45 QUAD (AMP 558503-1)

FIG. 12A

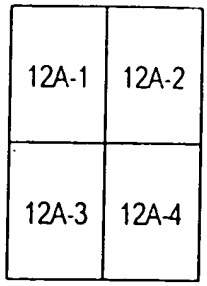
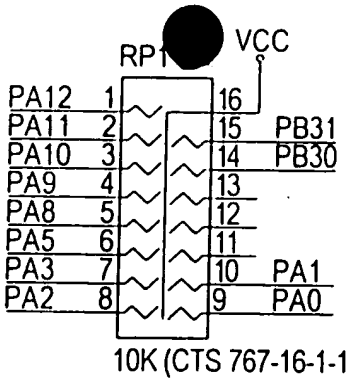
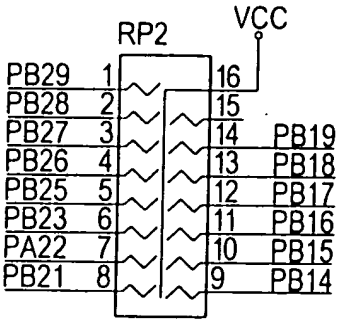


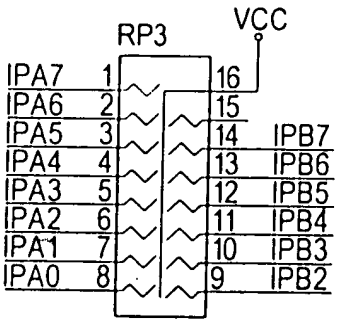
FIG. 12A-1



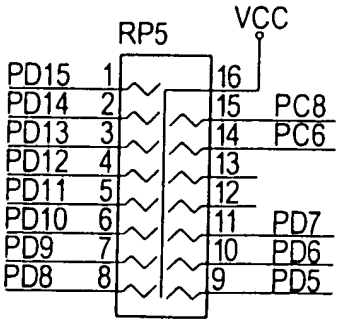
10K (CTS 767-16-1-103-JTR)



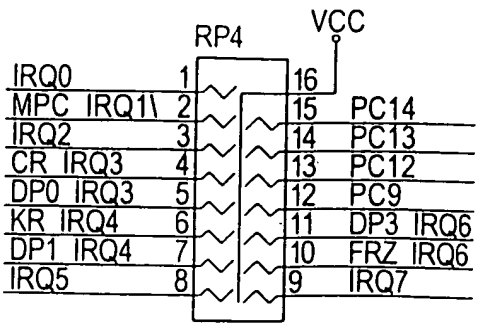
10K (CTS 767-16-1-103-JTR)



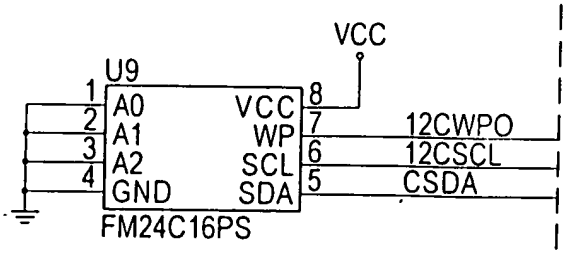
10K (CTS 767-16-1-103-JTR)



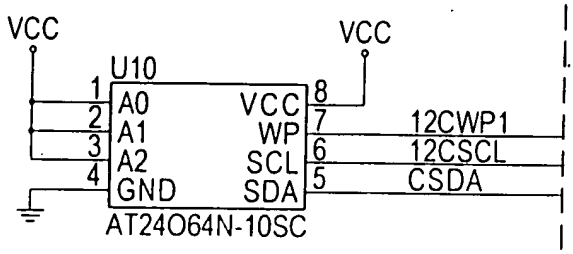
10K (CTS 767-16-1-103-JTR)



10K (CTS 767-16-1-103-JTR)



FM24C16PS



AT24O64N-10SC

PORTS A,B,C AND D DO NOT HAVE MPC860 INTERNAL PULLUP RESISTORS.

FIG. 12A-2

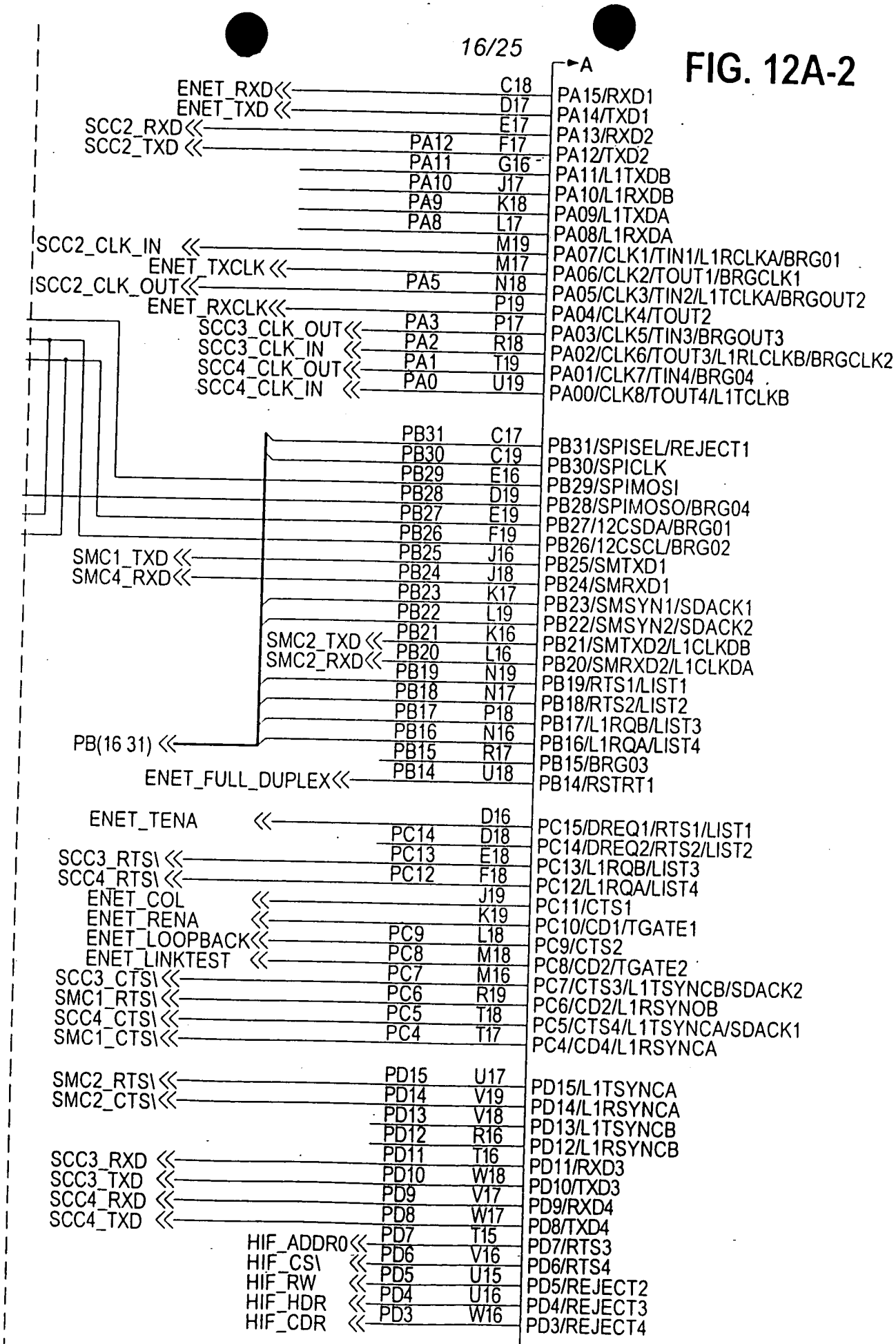
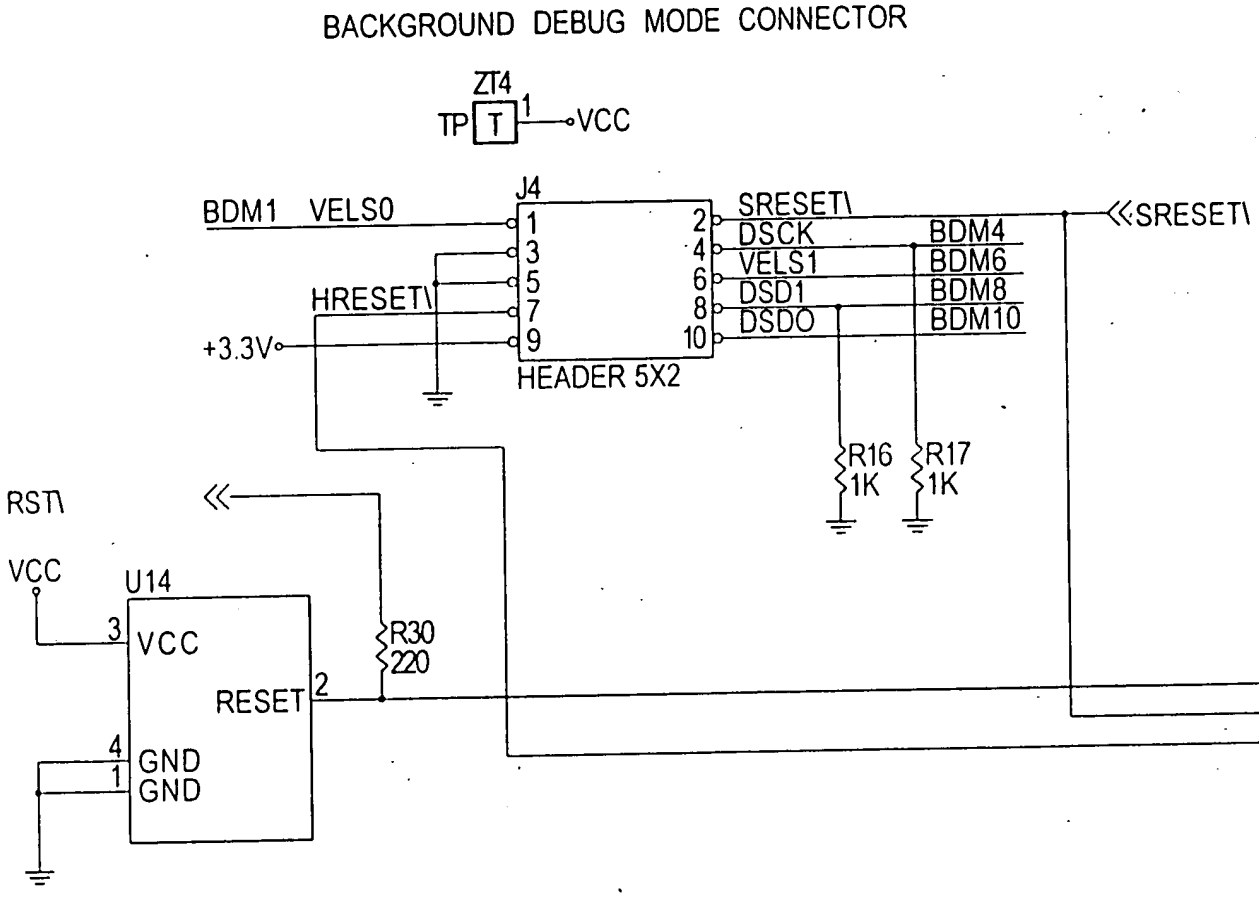

A
ENET_RXD
ENET_TXD
SCC2_RXD
SCC2_TXD
SCC2_CLK_IN
ENET_TXCLK
SCC2_CLK_OUT
ENET_RXCLK
SCC3_CLK_OUT
SCC3_CLK_IN
SCC4_CLK_OUT
SCC4_CLK_IN
SMC1_TXD
SMC4_RXD
SMC2_TXD
SMC2_RXD
PB(16 31)
ENET_FULL_DUPLEX
ENET_TENA
SCC3_RTS\
SCC4_RTS\
ENET_COL
ENET_RENA
ENET_LOOPBACK
ENET_LINKTEST
SCC3_CTS\
SMC1_RTS\
SCC4_CTS\
SMC1_CTS\
SMC2_RTS\
SMC2_CTS\
SCC3_RXD
SCC3_TXD
SCC4_RXD
SCC4_TXD
HIF_ADDR0
HIF_CS\
HIF_RW
HIF_HDR
HIF_CDR
C18 PA15/RXD1
D17 PA14/TXD1
E17 PA13/RXD2
PA12 F17 PA12/TXD2
PA11 G16 PA11/L1TXDB
PA10 J17 PA10/L1RXDB
PA9 K18 PA09/L1TXDA
PA8 L17 PA08/L1RXDA
M19 PA07/CLK1/TIN1/L1RCLKA/BRG01
M17 PA06/CLK2/TOUT1/BRGCLK1
PA5 N18 PA05/CLK3/TIN2/L1TCLKA/BRGOUT2
P19 PA04/CLK4/TOUT2
PA3 P17 PA03/CLK5/TIN3/BRGOUT3
PA2 R18 PA02/CLK6/TOUT3/L1RLCLKB/BRGCLK2
PA1 T19 PA01/CLK7/TIN4/BRG04
PA0 U19 PA00/CLK8/TOUT4/L1TCLKB
PB31 C17 PB31/SPISEL/REJECT1
PB30 C19 PB30/SPICLK
PB29 E16 PB29/SPIMOSI
PB28 D19 PB28/SPIMOSO/BRG04
PB27 E19 PB27/12CSDA/BRG01
PB26 F19 PB26/12CSCL/BRG02
PB25 J16 PB25/SMTXD1
PB24 J18 PB24/SMRXD1
PB23 K17 PB23/SMSYN1/SDACK1
PB22 L19 PB22/SMSYN2/SDACK2
PB21 K16 PB21/SMTXD2/L1CLKDB
PB20 L16 PB20/SMRXD2/L1CLKDA
PB19 N19 PB19/RTS1/LIST1
PB18 N17 PB18/RTS2/LIST2
PB17 P18 PB17/L1RQB/LIST3
PB16 N16 PB16/L1RQA/LIST4
PB15 R17 PB15/BRG03
PB14 U18 PB14/RSTRT1
D16 PC15/DREQ1/RTS1/LIST1
PC14 D18 PC14/DREQ2/RTS2/LIST2
PC13 E18 PC13/L1RQB/LIST3
PC12 F18 PC12/L1RQA/LIST4
J19 PC11/CTS1
K19 PC10/CD1/TGATE1
PC9 L18 PC9/CTS2
PC8 M18 PC8/CD2/TGATE2
PC7 M16 PC7/CTS3/L1TSYNCB/SDACK2
PC6 R19 PC6/CD2/L1RSYNOB
PC5 T18 PC5/CTS4/L1TSYNCA/SDACK1
PC4 T17 PC4/CD4/L1RSYNCA
PD15 U17 PD15/L1TSYNCA
PD14 V19 PD14/L1RSYNCA
PD13 V18 PD13/L1TSYNCB
PD12 R16 PD12/L1RSYNCB
PD11 T16 PD11/RXD3
PD10 W18 PD10/TXD3
PD9 V17 PD9/RXD4
PD8 W17 PD8/TXD4
PD7 T15 PD7/RTS3
PD6 V16 PD6/RTS4
PD5 U15 PD5/REJECT2
PD4 U16 PD4/REJECT3
PD3 W16 PD3/REJECT4

FIG. 12A-3


BACKGROUND DEBUG MODE CONNECTOR
ZT4
TP
T
1
VCC
J4
BDM1
VELS0
HRESET\
+3.3V
1
3
5
7
9
2
4
6
8
10
SRESET\
DSCK
VELS1
DSD1
DSDO
BDM4
BDM6
BDM8
BDM10
HEADER 5X2
SRESET\
R16
1K
R17
1K
RST\
VCC
U14
3
VCC
RESET
2
R30
220
4
GND
1
GND

PCMCIA PORT IPA IS USED FOR A HARDWARE REVISION REGISTER WHICH IS READ BY SOFTWARE. EACH TIME THE BOARD IS REVISED THE VALUE SHOULD BE INCREMENTED.

IPB7 CONFIGURED AS AT3
IPB6 CONFIGURED AS AT0
IPB5 CONFIGURED AS VF1
IPB4 CONFIGURED AS VF0
IPB3 CONFIGURED AS VF2
IPB2 CONFIGURED AS AT2

FIG. 12A-4

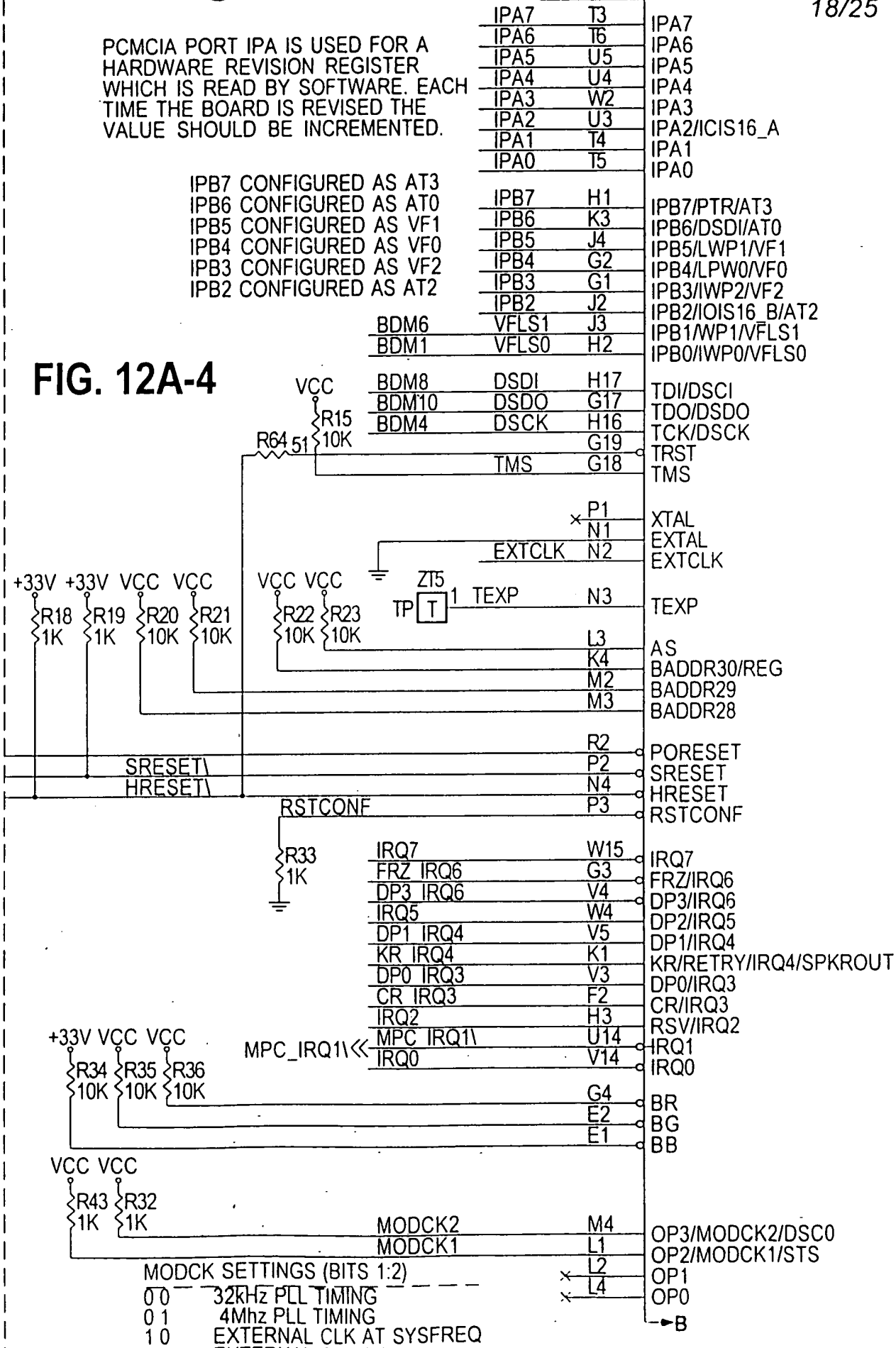


FIG. 12B

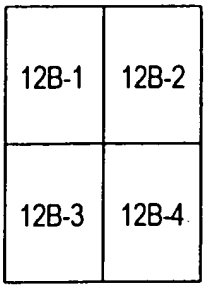
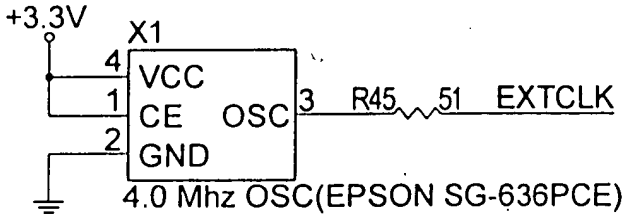
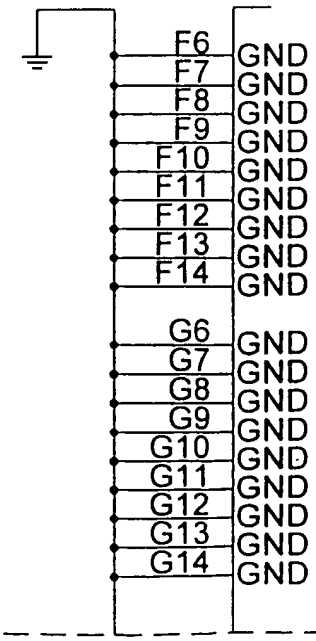


FIG. 12B-1





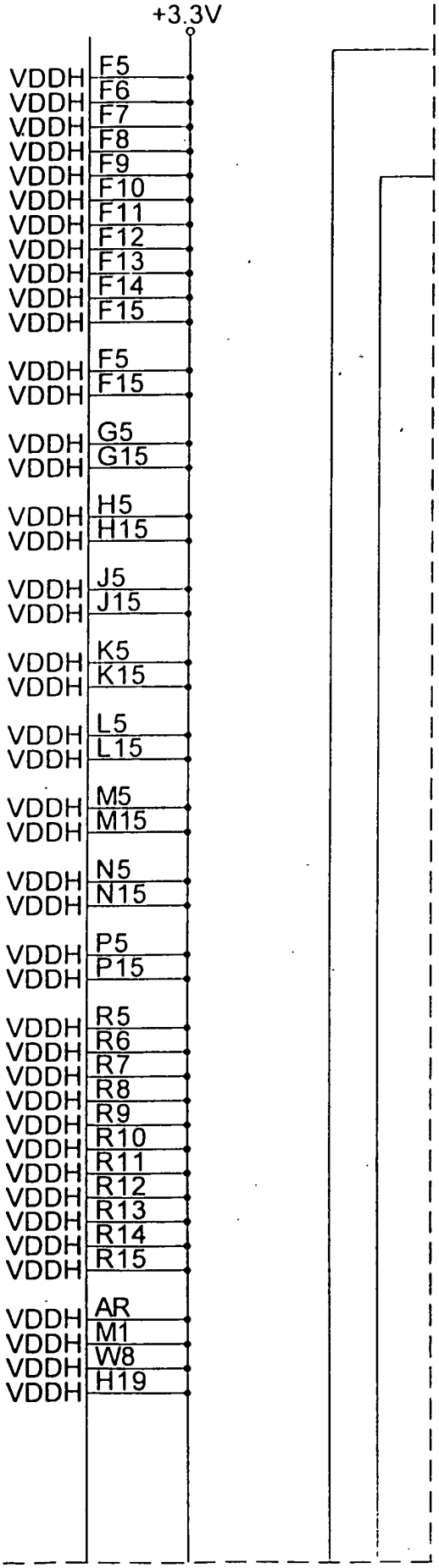
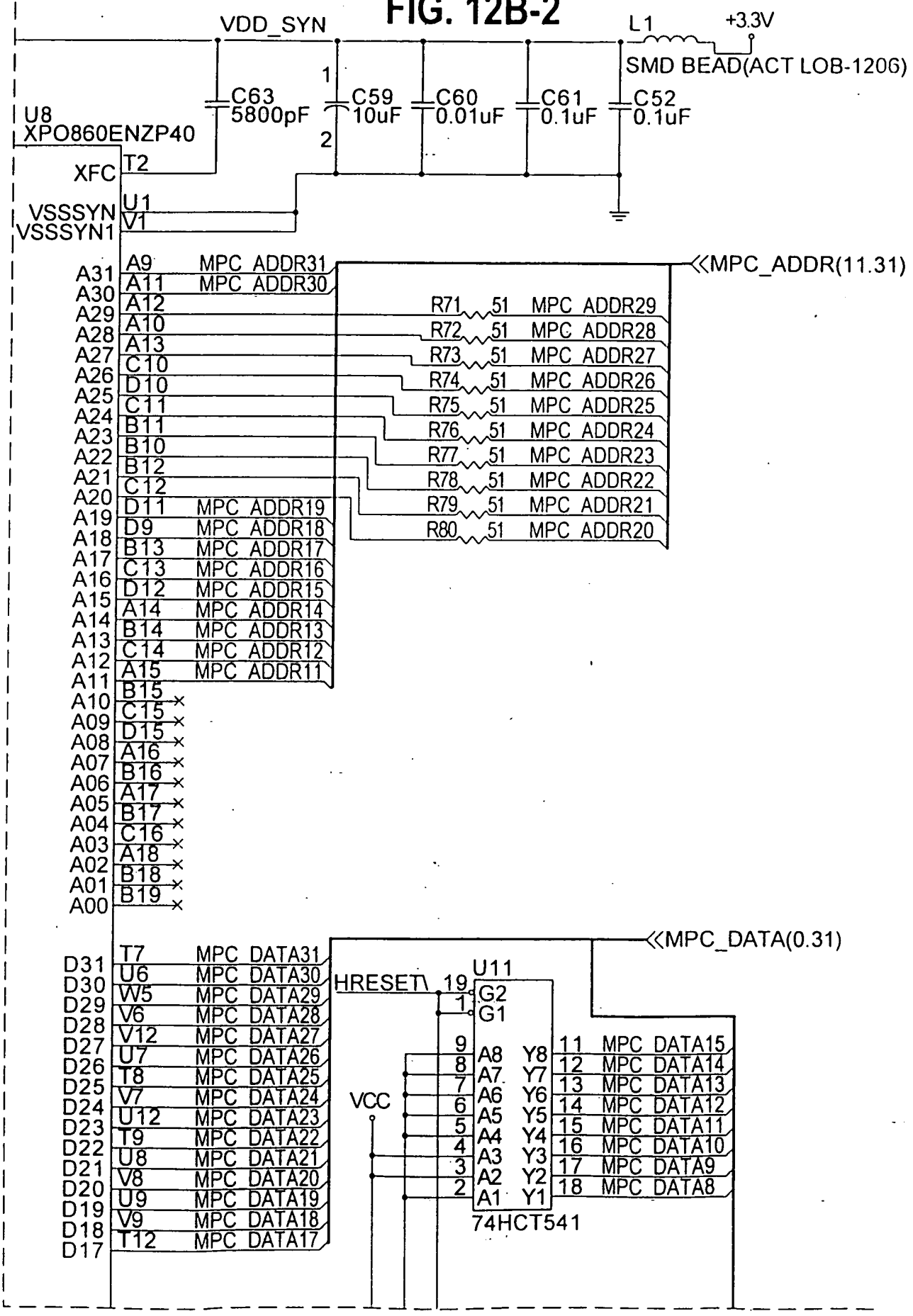


FIG. 12B-2


VDD_SYN
L1
+3.3V
SMD BEAD(ACT LOB-1206)
C63 5800pF
C59 10uF
C60 0.01uF
C61 0.1uF
C52 0.1uF
U8
XPO860ENZP40
XFC T2
VSSSYN U1
VSSSYN1 V1
A31 A9 MPC ADDR31
A30 A11 MPC ADDR30
A29 A12
A28 A10
A27 A13
A26 C10
A25 D10
A24 C11
A23 B11
A22 B10
A21 B12
A20 C12
A19 D11 MPC ADDR19
A18 D9 MPC ADDR18
A17 B13 MPC ADDR17
A16 C13 MPC ADDR16
A15 D12 MPC ADDR15
A14 A14 MPC ADDR14
A13 B14 MPC ADDR13
A12 C14 MPC ADDR12
A11 A15 MPC ADDR11
A10 B15
A09 C15
A08 D15
A07 A16
A06 B16
A05 A17
A04 B17
A03 C16
A02 A18
A01 B18
A00 B19
R71 51 MPC ADDR29
R72 51 MPC ADDR28
R73 51 MPC ADDR27
R74 51 MPC ADDR26
R75 51 MPC ADDR25
R76 51 MPC ADDR24
R77 51 MPC ADDR23
R78 51 MPC ADDR22
R79 51 MPC ADDR21
R80 51 MPC ADDR20
≪MPC_ADDR(11.31)
≪MPC_DATA(0.31)
D31 T7 MPC DATA31
D30 U6 MPC DATA30
D29 W5 MPC DATA29
D28 V6 MPC DATA28
D27 V12 MPC DATA27
D26 U7 MPC DATA26
D25 T8 MPC DATA25
D24 V7 MPC DATA24
D23 U12 MPC DATA23
D22 T9 MPC DATA22
D21 U8 MPC DATA21
D20 V8 MPC DATA20
D19 U9 MPC DATA19
D18 V9 MPC DATA18
D17 T12 MPC DATA17
HRESET\
U11
19 G2
1 G1
VCC
9 A8 Y8 11 MPC DATA15
8 A7 Y7 12 MPC DATA14
7 A6 Y6 13 MPC DATA13
6 A5 Y5 14 MPC DATA12
5 A4 Y4 15 MPC DATA11
4 A3 Y3 16 MPC DATA10
3 A2 Y2 17 MPC DATA9
2 A1 Y1 18 MPC DATA8
74HCT541

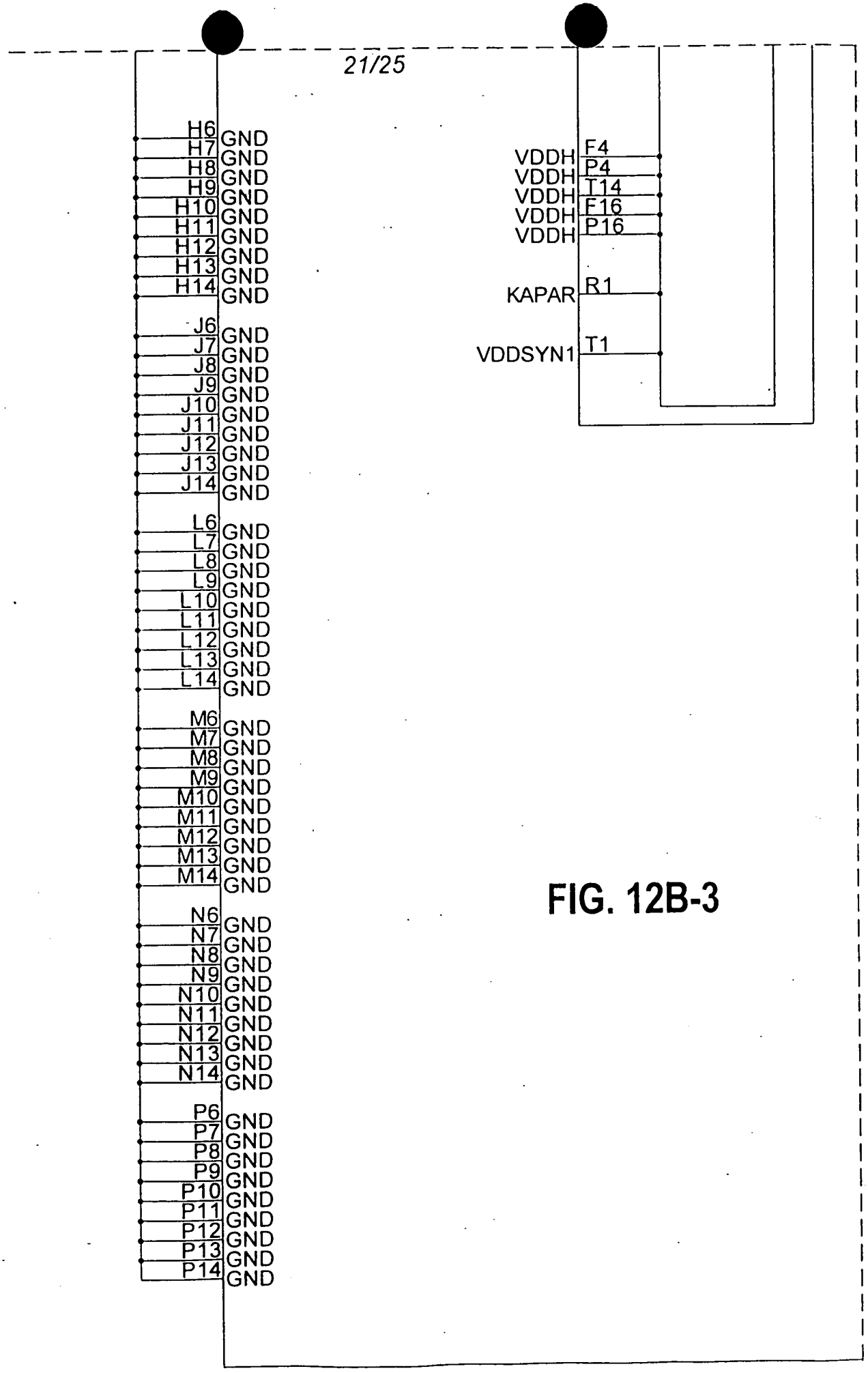

H6 GND
H7 GND
H8 GND
H9 GND
H10 GND
H11 GND
H12 GND
H13 GND
H14 GND
J6 GND
J7 GND
J8 GND
J9 GND
J10 GND
J11 GND
J12 GND
J13 GND
J14 GND
L6 GND
L7 GND
L8 GND
L9 GND
L10 GND
L11 GND
L12 GND
L13 GND
L14 GND
M6 GND
M7 GND
M8 GND
M9 GND
M10 GND
M11 GND
M12 GND
M13 GND
M14 GND
N6 GND
N7 GND
N8 GND
N9 GND
N10 GND
N11 GND
N12 GND
N13 GND
N14 GND
P6 GND
P7 GND
P8 GND
P9 GND
P10 GND
P11 GND
P12 GND
P13 GND
P14 GND
VDDH F4
VDDH P4
VDDH T14
VDDH F16
VDDH P16
KAPAR R1
VDDSYN1 T1

FIG. 12B-3

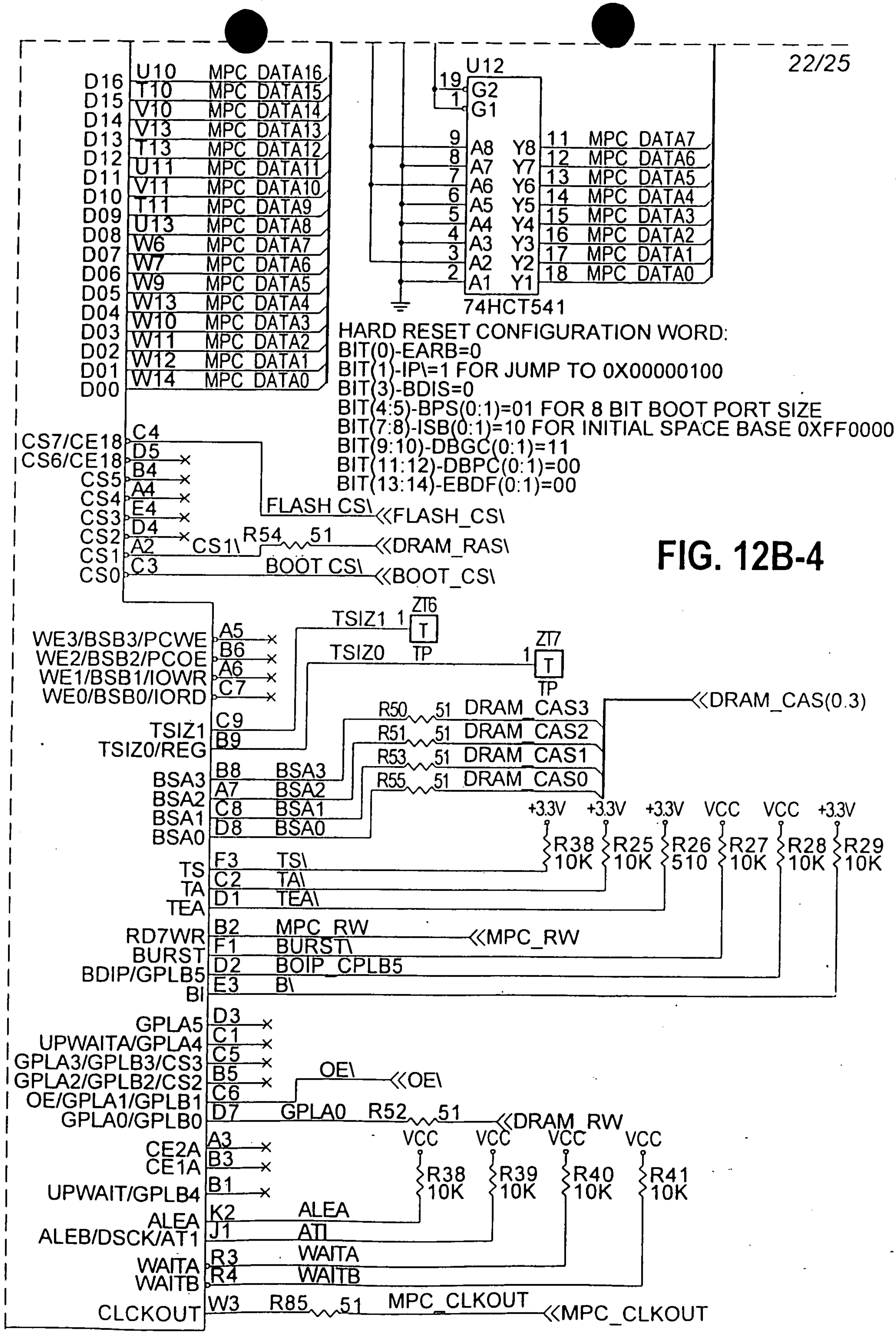

U12
19 G2
1 G1
9 A8 Y8 11 MPC DATA7
8 A7 Y7 12 MPC DATA6
7 A6 Y6 13 MPC DATA5
6 A5 Y5 14 MPC DATA4
5 A4 Y4 15 MPC DATA3
4 A3 Y3 16 MPC DATA2
3 A2 Y2 17 MPC DATA1
2 A1 Y1 18 MPC DATA0
74HCT541
D16 U10 MPC DATA16
D15 T10 MPC DATA15
D14 V10 MPC DATA14
D13 V13 MPC DATA13
D12 T13 MPC DATA12
D11 U11 MPC DATA11
D10 V11 MPC DATA10
D09 T11 MPC DATA9
D08 U13 MPC DATA8
D07 W6 MPC DATA7
D06 W7 MPC DATA6
D05 W9 MPC DATA5
D04 W13 MPC DATA4
D03 W10 MPC DATA3
D02 W11 MPC DATA2
D01 W12 MPC DATA1
D00 W14 MPC DATA0
HARD RESET CONFIGURATION WORD:
BIT(0)-EARB=0
BIT(1)-IP\=1 FOR JUMP TO 0X00000100
BIT(3)-BDIS=0
BIT(4:5)-BPS(0:1)=01 FOR 8 BIT BOOT PORT SIZE
BIT(7:8)-ISB(0:1)=10 FOR INITIAL SPACE BASE 0XFF0000
BIT(9:10)-DBGC(0:1)=11
BIT(11:12)-DBPC(0:1)=00
BIT(13:14)-EBDF(0:1)=00
CS7/CE18 C4
CS6/CE18 D5
CS5 B4
CS4 A4
CS3 E4
CS2 D4
CS1 A2
CS0 C3
FLASH CS\
<<FLASH_CS\
CS1\ R54 51
<<DRAM_RAS\
BOOT CS\
<<BOOT_CS\
WE3/BSB3/PCWE A5
WE2/BSB2/PCOE B6
WE1/BSB1/IOWR A6
WE0/BSB0/IORD C7
TSIZ1 1
ZT6
T
TP
TSIZ0
ZT7
T
TP
TSIZ1 C9
TSIZ0/REG B9
R50 51 DRAM CAS3
R51 51 DRAM CAS2
R53 51 DRAM CAS1
R55 51 DRAM CAS0
<<DRAM_CAS(0.3)
BSA3 B8 BSA3
BSA2 A7 BSA2
BSA1 C8 BSA1
BSA0 D8 BSA0
+3.3V +3.3V +3.3V VCC VCC +3.3V
R38 10K
R25 10K
R26 510
R27 10K
R28 10K
R29 10K
TS F3 TS\
TA C2 TA\
TEA D1 TEA\
RD7WR B2 MPC_RW
<<MPC_RW
BURST F1 BURST\
BDIP/GPLB5 D2 BOIP_CPLB5
BI E3 B\
GPLA5 D3
UPWAITA/GPLA4 C1
GPLA3/GPLB3/CS3 C5
GPLA2/GPLB2/CS2 B5
OE\
<<OE\
OE/GPLA1/GPLB1 C6
GPLA0/GPLB0 D7 GPLA0 R52 51
<<DRAM_RW
CE2A A3
CE1A B3
UPWAIT/GPLB4 B1
VCC VCC VCC VCC
R38 10K
R39 10K
R40 10K
R41 10K
ALEA K2 ALEA
ALEB/DSCK/AT1 J1 ATI
WAITA R3 WAITA
WAITB R4 WAITB
CLCKOUT W3 R85 51 MPC_CLKOUT
<<MPC_CLKOUT

FIG. 12B-4

FIG. 13

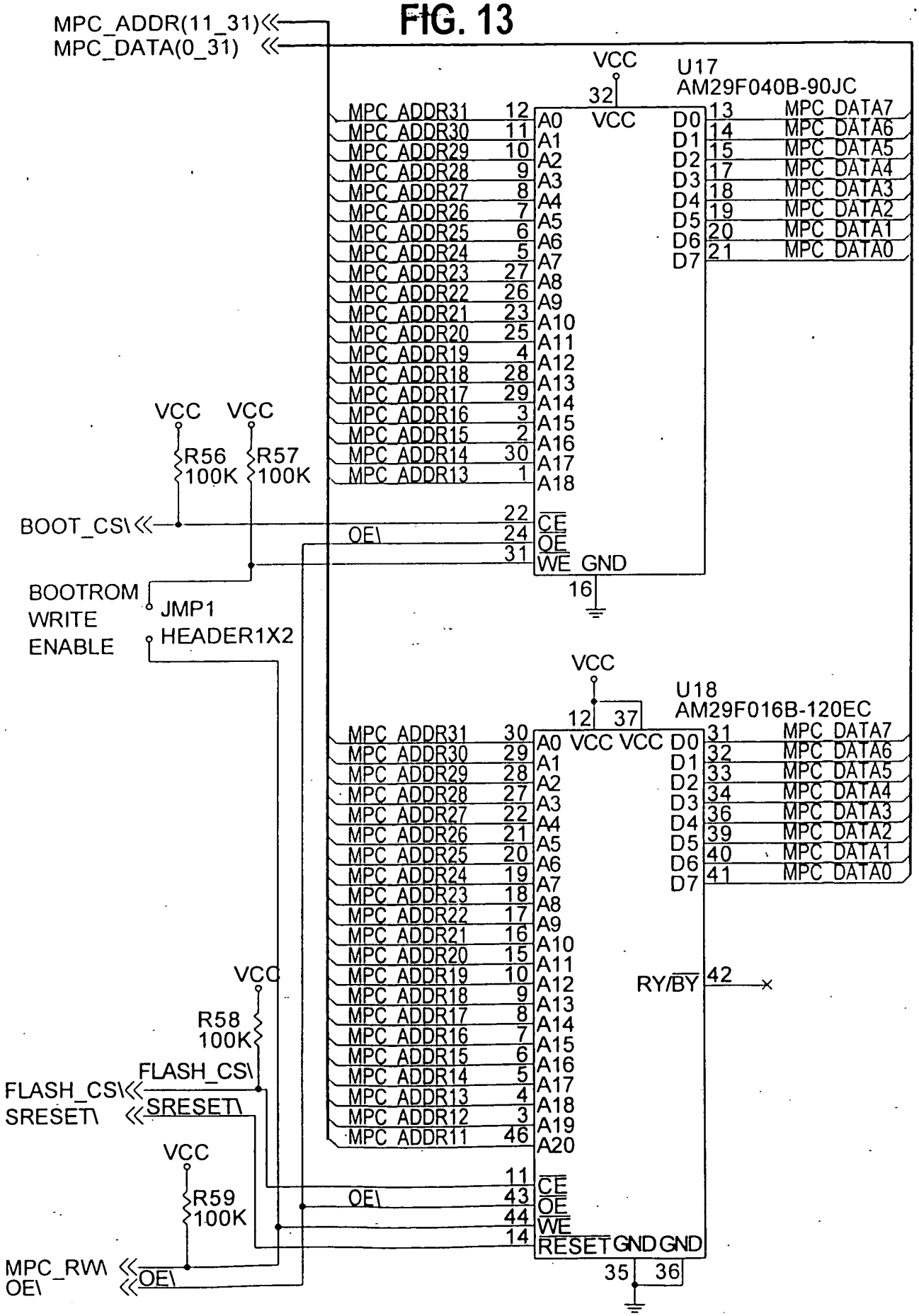

MPC_ADDR(11_31)
MPC_DATA(0_31)
VCC
U17
AM29F040B-90JC
32
VCC
MPC_ADDR31 12 A0
MPC_ADDR30 11 A1
MPC_ADDR29 10 A2
MPC_ADDR28 9 A3
MPC_ADDR27 8 A4
MPC_ADDR26 7 A5
MPC_ADDR25 6 A6
MPC_ADDR24 5 A7
MPC_ADDR23 27 A8
MPC_ADDR22 26 A9
MPC_ADDR21 23 A10
MPC_ADDR20 25 A11
MPC_ADDR19 4 A12
MPC_ADDR18 28 A13
MPC_ADDR17 29 A14
MPC_ADDR16 3 A15
MPC_ADDR15 2 A16
MPC_ADDR14 30 A17
MPC_ADDR13 1 A18
D0 13 MPC_DATA7
D1 14 MPC_DATA6
D2 15 MPC_DATA5
D3 17 MPC_DATA4
D4 18 MPC_DATA3
D5 19 MPC_DATA2
D6 20 MPC_DATA1
D7 21 MPC_DATA0
VCC VCC
R56 100K
R57 100K
BOOT_CS\
22 CE
OE\ 24 OE
31 WE
GND 16
BOOTROM WRITE ENABLE
JMP1 HEADER1X2
VCC
U18
AM29F016B-120EC
12 37
VCC VCC
MPC_ADDR31 30 A0
MPC_ADDR30 29 A1
MPC_ADDR29 28 A2
MPC_ADDR28 27 A3
MPC_ADDR27 22 A4
MPC_ADDR26 21 A5
MPC_ADDR25 20 A6
MPC_ADDR24 19 A7
MPC_ADDR23 18 A8
MPC_ADDR22 17 A9
MPC_ADDR21 16 A10
MPC_ADDR20 15 A11
MPC_ADDR19 10 A12
MPC_ADDR18 9 A13
MPC_ADDR17 8 A14
MPC_ADDR16 7 A15
MPC_ADDR15 6 A16
MPC_ADDR14 5 A17
MPC_ADDR13 4 A18
MPC_ADDR12 3 A19
MPC_ADDR11 46 A20
D0 31 MPC_DATA7
D1 32 MPC_DATA6
D2 33 MPC_DATA5
D3 34 MPC_DATA4
D4 36 MPC_DATA3
D5 39 MPC_DATA2
D6 40 MPC_DATA1
D7 41 MPC_DATA0
RY/BY 42
VCC
R58 100K
FLASH_CS\
FLASH_CS\
SRESET\
SRESET\
VCC
R59 100K
11 CE
OE\ 43 OE
44 WE
14 RESET
GND GND
35 36
MPC_RW\
OE\
OE\

FIG. 14

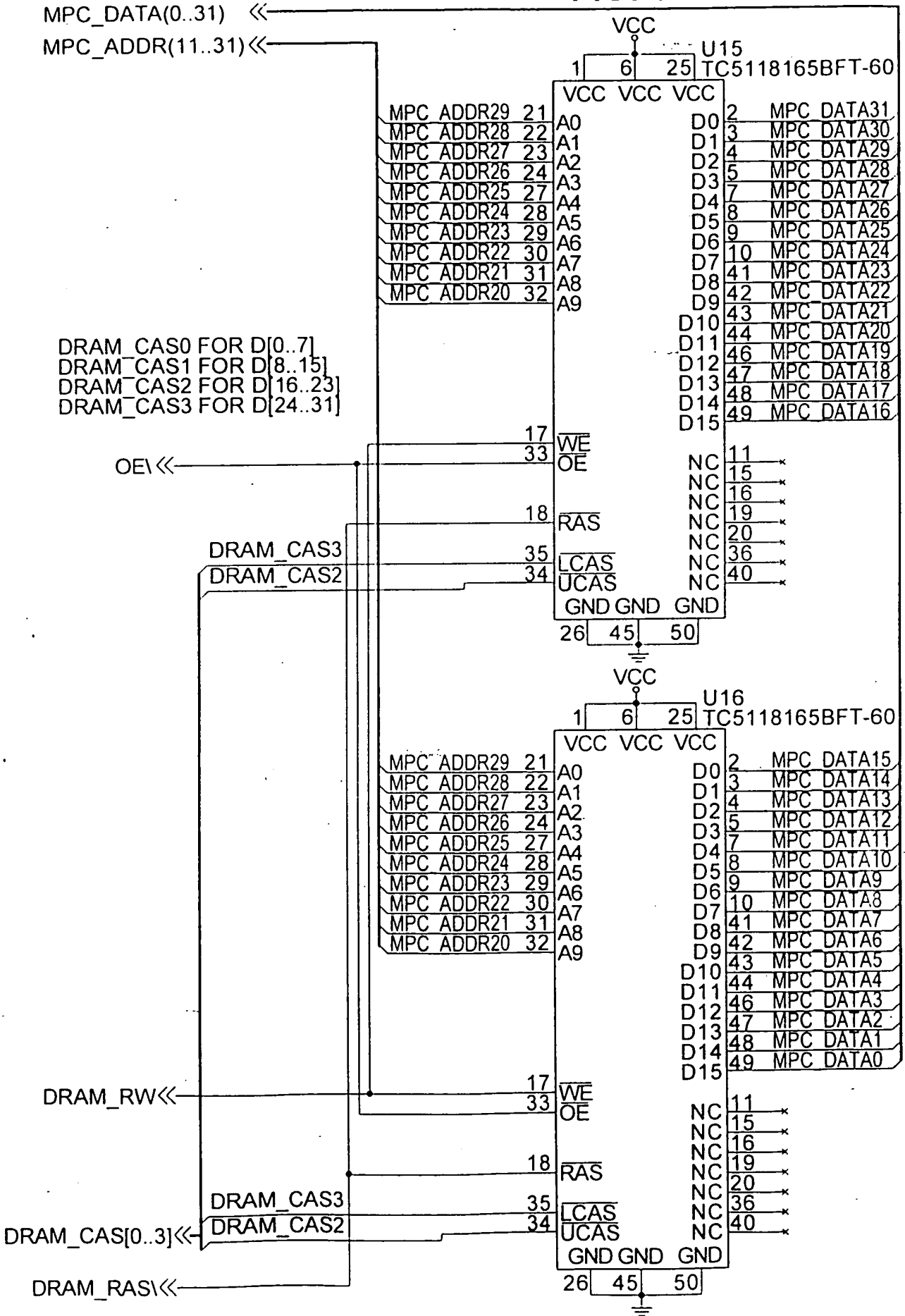
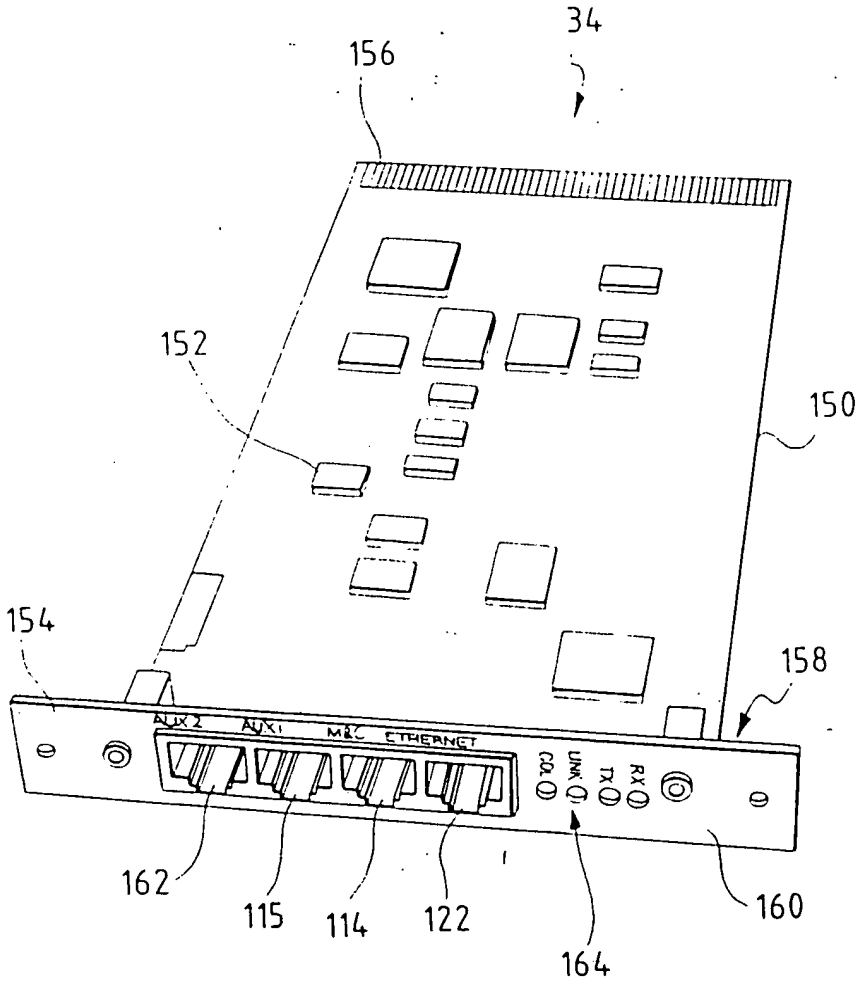

MPC_DATA(0..31)
MPC_ADDR(11..31)
VCC
U15
TC5118165BFT-60
VCC VCC VCC
MPC_ADDR29 21 A0
MPC_ADDR28 22 A1
MPC_ADDR27 23 A2
MPC_ADDR26 24 A3
MPC_ADDR25 27 A4
MPC_ADDR24 28 A5
MPC_ADDR23 29 A6
MPC_ADDR22 30 A7
MPC_ADDR21 31 A8
MPC_ADDR20 32 A9
D0 2 MPC_DATA31
D1 3 MPC_DATA30
D2 4 MPC_DATA29
D3 5 MPC_DATA28
D4 7 MPC_DATA27
D5 8 MPC_DATA26
D6 9 MPC_DATA25
D7 10 MPC_DATA24
D8 41 MPC_DATA23
D9 42 MPC_DATA22
D10 43 MPC_DATA21
D11 44 MPC_DATA20
D12 46 MPC_DATA19
D13 47 MPC_DATA18
D14 48 MPC_DATA17
D15 49 MPC_DATA16
DRAM_CAS0 FOR D[0..7]
DRAM_CAS1 FOR D[8..15]
DRAM_CAS2 FOR D[16..23]
DRAM_CAS3 FOR D[24..31]
17 WE
33 OE
OE\
18 RAS
DRAM_CAS3
DRAM_CAS2
35 LCAS
34 UCAS
NC 11
NC 15
NC 16
NC 19
NC 20
NC 36
NC 40
GND GND GND
26 45 50
VCC
U16
TC5118165BFT-60
VCC VCC VCC
MPC_ADDR29 21 A0
MPC_ADDR28 22 A1
MPC_ADDR27 23 A2
MPC_ADDR26 24 A3
MPC_ADDR25 27 A4
MPC_ADDR24 28 A5
MPC_ADDR23 29 A6
MPC_ADDR22 30 A7
MPC_ADDR21 31 A8
MPC_ADDR20 32 A9
D0 2 MPC_DATA15
D1 3 MPC_DATA14
D2 4 MPC_DATA13
D3 5 MPC_DATA12
D4 7 MPC_DATA11
D5 8 MPC_DATA10
D6 9 MPC_DATA9
D7 10 MPC_DATA8
D8 41 MPC_DATA7
D9 42 MPC_DATA6
D10 43 MPC_DATA5
D11 44 MPC_DATA4
D12 46 MPC_DATA3
D13 47 MPC_DATA2
D14 48 MPC_DATA1
D15 49 MPC_DATA0
DRAM_RW
17 WE
33 OE
18 RAS
DRAM_CAS3
DRAM_CAS2
DRAM_CAS[0..3]
35 LCAS
34 UCAS
NC 11
NC 15
NC 16
NC 19
NC 20
NC 36
NC 40
GND GND GND
26 45 50
DRAM_RAS\

FIG. 15


34
156
152
150
154
158
AUX 2
AUX 1
M&C
ETHERNET
COL
LINK
TX
RX
162
115
114
122
164
160